Suppression of DC Link Voltage Fluctuation and Dynamic Response Optimization in Grid-Tied Inverters

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Abstract: During operation, the DC bus in single-phase power conversion systems inevitably generates double-frequency voltage ripple. To address the issue of current reference tracking accuracy, it is common practice in engineering to embed notch filters within the control algorithm. However, traditional solutions suffer from inherent drawbacks such as sluggish dynamic response and a tendency for system oscillations. This paper innovatively proposes a real-time computational algorithm based on system parameters to identify the second harmonic voltage component. This approach requires neither modifications to the main circuit topology nor additional filtering stages in the voltage loop. By redesigning the voltage outer loop controller structure, the dynamic response characteristics of the system are significantly enhanced, effectively suppressing overshoot during voltage regulation. Combined with a current inner loop control strategy employing a quasi-proportional resonant regulator, the constructed dual closed-loop control system achieves excellent dynamic performance and stability while maintaining steady-state precision. Simulation results based on MATLAB /Simulink confirm the feasibility and superiority of the proposed control scheme.

Keywords: Harmonic Voltage Identification; Dual Closed-loop Control; Quasi-Proportional Resonant Control; Dynamic Performance; Second Harmonic Suppression

1. Introduction

Single-phase inverters, serving as core components in power electronic systems, play an indispensable role in critical fields such as renewable energy generation, industrial drives, and uninterruptible power supplies [1-2]. With the ongoing global energy transition and continuous innovation in power electronics technology, modern power systems are imposing increasingly stringent performance requirements on inverters. These diverse industrial applications demand not only precise control of voltage, current, and power but also excellent dynamic response characteristics and steady-state performance under complex operating conditions, while simultaneously requiring compliance with rigorous technical specifications including high efficiency, high power density, and low electromagnetic interference. Particularly driven by current carbon neutrality goals, single-phase inverters must also demonstrate higher levels of intelligence and enhanced grid adaptability to meet the construction needs of future smart grids. However, single-phase inverters consistently face a long-standing technical challenge during operation: significant twice-line-frequency harmonic components with considerable amplitude are generated on the DC bus due to the inherent instantaneous power pulsation characteristics of single-phase systems [3-4]. The physical essence of this problem lies in the inherent periodic fluctuation of power transfer in single-phase systems. The mathematical model established by Jiang et al. [5] provides in-depth theoretical analysis and quantitative research on this phenomenon, clearly identifying this power pulsation characteristic as the fundamental cause of current and voltage ripple at twice the line frequency on the DC side. If these harmonic components are not effectively suppressed, they can exert multiple adverse effects on the system's output characteristics through the control loop, leading not only to output waveform distortion and degraded power quality but also potentially causing electromagnetic interference issues, increasing system losses, and reducing conversion efficiency. Particularly noteworthy is the systematic experimental validation by Zhou et al. [6], which demonstrates that such second-harmonic components may induce system resonance under specific

conditions. When system impedance characteristics match the harmonic frequency, resonance phenomena occur, causing a sharp increase in harmonic amplitude that further amplifies the threat to system stability, presenting severe challenges to the secure operation of the system.

To address the issue of second-order harmonics on the DC side, the academic community has proposed various solutions, which can be broadly categorized into two technical pathways: suppression methods based on improvements in hardware topology and suppression strategies based on optimization of control algorithms. In terms of hardware improvements, Alsolami et al. [7] proposed a design scheme using auxiliary circuits, which constructs a harmonic current path by adding an LC filter network, but this method significantly increases system volume and cost; Li et al. [8] introduced a differential capacitor solution that achieves complementary capacitor voltage ripple, yet due to uncontrollable intervals in the algorithm, it cannot achieve full-cycle effective suppression. In the field of control algorithm optimization, Somkun et al. [9] employed a notch filter for harmonic suppression, but it introduces phase lag issues; Ahangarkolaei et al. [10] applied predictive control to harmonic suppression, achieving notable results but exhibiting sensitivity to parameter variations; and for two-stage single-phase inverters, the virtual fractional-order inductance control proposed by Zhou et al. [11-12] effectively eliminates second-order harmonic current but inevitably reduces the system's dynamic response performance.

Building on an in-depth analysis of existing control strategies, this paper proposes a composite control strategy combining quasi-proportional resonant control with an improved voltage feedforward method. This solution first establishes an accurate mathematical model of the system to analyze the generation mechanism and propagation path of the second-order harmonics. Subsequently, a quasi-proportional resonant controller is adopted for the inner current loop, leveraging its high-gain characteristics at the fundamental frequency to achieve precise tracking of reference signals. Meanwhile, a harmonic extraction algorithm based on instantaneous power calculation is introduced into the outer voltage loop to estimate the second-order harmonic components in real time and implement feedforward compensation.

2. Traditional Control Strategy

The main circuit of a single-phase inverter is shown in Figure 1, where U_d, P_d, and C_d represent the DC-side voltage, power, and filter capacitor respectively; the AC filter inductor and capacitor are L and C, and the grid voltage is U_g; P_c and P_g indicate the power flowing through the capacitor and the grid.

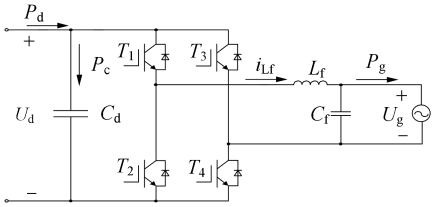


Figure 1. Main Circuit Topology

2.1 Current Inner Loop Design

To enhance the stability and anti-interference performance of the control system, this paper adopts a quasi-PR regulator as the current loop controller with the following transfer function:

$$T_{PR}(s) = k_p + \frac{2k_r\omega_t s}{s^2 + 2\omega_t s + \omega_n^2} \quad (1)$$

where k_p is the proportionality coefficient, k_r is the resonance coefficient, ω_n is the fundamental angular frequency, and ω_t is the cutoff frequency, ω_t=5rad/s, k_p=0.015, k_r=8, and $\omega_0=2\pi f_0 =100\pi$.

The inner current loop is shown in Figure 2, where $K = 1/U_d$.

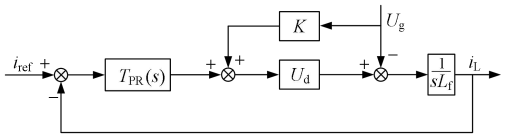


Figure 2. Current Inner Loop Control

2.2 Voltage Outer Loop Design

The control block diagram of the outer voltage loop is shown in Figure 3, where U_{dref} is the voltage reference setpoint, k_{dc} and τ are the Pregulator parameters, $G_c(s)$ is the closed-loop transfer function of the inner current loop.

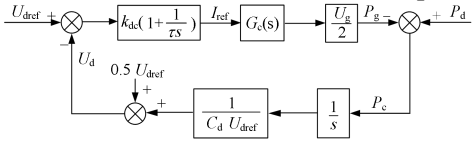


Figure 3. Voltage Outer Loop Control

3. Improved DC Voltage Control Strategy

3.1 Control Strategy

The time-domain characteristics of the DC bus

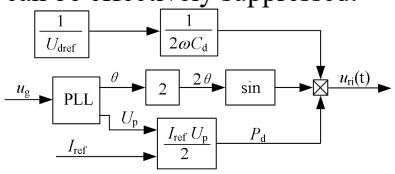
voltage can be described by Equation 3, where u_{ri} (t) represents the second-harmonic voltage ripple. Given the inherent double-frequency ripple characteristic in the DC bus voltage and its measurability, the estimated value of the ripple component can be obtained through analytical methods:

$$\begin{aligned} U_{\mathrm{d}} &= u_{\mathrm{d}}(t) - u_{\mathrm{ri}}(t) \\ &= u_{\mathrm{d}}(t) - \frac{P_{\mathrm{d}}}{2\omega C_{\mathrm{d}} U_{\mathrm{dref}}} \sin 2\theta \end{aligned} \tag{2}$$

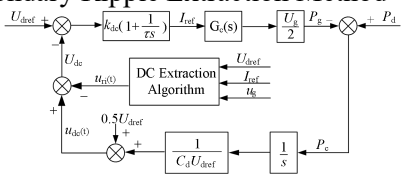
If system losses are ignored, P_d is equal to P_g. The current loop can rapidly and accurately track the system's output value. When the grid-side current reference amplitude I_{ref} is used to characterize the actual grid-side current, and the voltage amplitude U_p from the phase-locked loop is employed to represent the actual grid-side voltage, the following relationship can be established:

$$P_{\mathrm{d}} = \frac{U_{\mathrm{p}} I_{\mathrm{ref}}}{2} \tag{3}$$

Based on the aforementioned analysis, the second harmonic component in the DC voltage can be extracted using the algorithm illustrated in Figure 4(a), with its implementation structure shown in Figure 4(b). By injecting a compensating signal with opposite phase to this second harmonic into the voltage outer-loop control, the harmonic fluctuation in the DC bus voltage can be effectively suppressed.



(a) Secondary Ripple Extraction Method



(b) Voltage Loop Control Diagram

Figure 4. Improved DC voltage Control Strategy

3.2 Parameter Design

Based on the block diagram presented in Figure 4, the characteristic equation for the complete control loop utilizing the proposed improved algorithm can be derived as:

$$1 - k_{\mathrm{dc}} \frac{U_{\mathrm{g}}}{2C_{\mathrm{d}}U_{\mathrm{dref}}} \left(1 + \frac{1}{\tau s}\right) \frac{1}{s} G_{\mathrm{c}}(s) = 0 \tag{4}$$

The closed-loop transfer function is:

$$G_{\mathrm{u}}(s) = \frac{\dfrac{1}{C_{\mathrm{d}}U_{\mathrm{dref}}} \dfrac{1}{s}}{1 - k_{\mathrm{dc}} \dfrac{U_{\mathrm{g}}}{2C_{\mathrm{d}}U_{\mathrm{dref}}} \left(1 + \dfrac{1}{\tau s}\right) \dfrac{1}{s} G_{\mathrm{c}}(s)} \tag{5}$$

To optimize the suppression of DC bus voltage fluctuations, it is theoretically necessary to reduce the value of τ to extend the voltage outer loop bandwidth. A root locus analysis was performed based on Equation (4) for four parameter configurations: τ = 12.5ms, 10ms, 7.5ms, and 5ms. Figure 5 demonstrates that as the value of τ decreases, the system remains stable while the intersection point of the root locus with the real axis gradually shifts leftward. Taking into account both dynamic performance and stability, τ = 5ms was ultimately determined to be the optimal parameter.

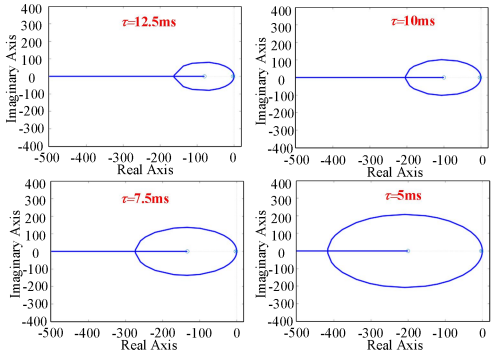


Figure 5. Root Trajectories of the Improved Control Algorithm for Different Values of τ

When the damping ratio ξ varies within the range of 0.1 to 0.8, the value of the controller parameter k_{dc} significantly influences the dynamic response characteristics of the system. The pole-zero distribution of the improved control algorithm model constructed based on Equation (5) is shown in Figure 6. Simulation results indicate that as the value of ξ increases, the dominant poles of the system continuously migrate toward the left half-plane, while the corresponding k_{dc} parameter exhibits a monotonically increasing characteristic. It should be noted that excessively high k_{dc} values amplify high-frequency system noise, adversely affecting the practical implementation of the controller. Furthermore, to ensure sufficient damping capability in the high-frequency range, the value of ξ should not be set too low. Through comprehensive optimization, ξ = 0.707 was selected as the optimal operating point, with a corresponding k_{dc} = 0.21. Under this parameter combination, the calculated system overshoot using the higher-order system approximation method is 11.3%, with a settling time of 23 ms.

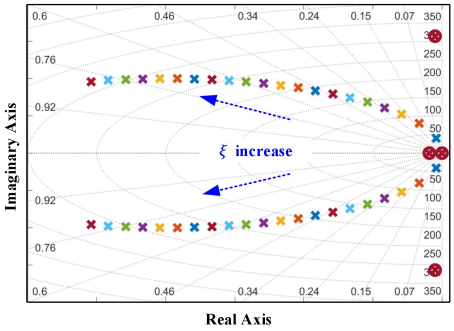


Figure 6. Closed-Loop Zero-Pole Distribution

4. Experimental Verification

To validate the control performance of the improved DC bus voltage extraction algorithm, this study established a numerical model of a single-phase H-bridge converter in the MATLAB/Simulink environment, with specific experimental parameters provided in Table 1. The algorithm was evaluated through two typical operational scenarios: first, examining the system dynamic response characteristics through step changes in the DC voltage reference; second, analyzing the voltage outer-loop response characteristics and grid-connected current stability under step disturbances in grid-side power.

Table 1. Experimental Platform Parameters

Variable Name	Variable symbol	Variable value
switching frequency	f_w	10kHz
grid frequency	f_l	50Hz
DC bus voltage	U_d	400V
RMS grid voltage	U_g	220V
filter inductors	L_f	0.6mH
filter capacitor	C_f	10uF
DC-side capacitance	C_d	220uF

4.1 DC Voltage Step Test

Figure 7 illustrates the first experimental scenario, where the DC bus voltage undergoes step-up transitions from 400V to 500V and step-down transitions from 500V to 400V. The measured settling times of the improved algorithm during voltage ascent are 22.3ms and 26.2ms, showing good agreement with the theoretical calculation of 23ms.

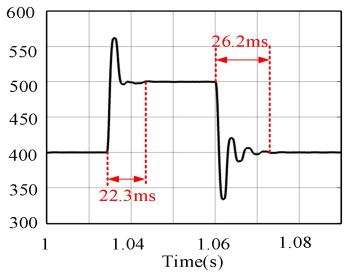


Figure 7. DC Bus Voltage Step Response Test

As shown in Figure 8, the second experimental scenario involves step changes of grid-side output power between 0kW and 10kW to verify the system's suppression capability against double-frequency ripple in the DC bus voltage and its dynamic response characteristics. The 10kW grid-side power output is achieved by connecting a 16Ω load to the DC side while maintaining a stable DC bus voltage of 400V. Experimental results demonstrate that the improved algorithm yields settling times of 23.4ms and 20.1ms during power step-up phases, consistent with the theoretical value of 23ms. Comparative analysis with the baseline control strategy confirms that the proposed improved control method effectively suppresses double-frequency voltage oscillations on the DC side.

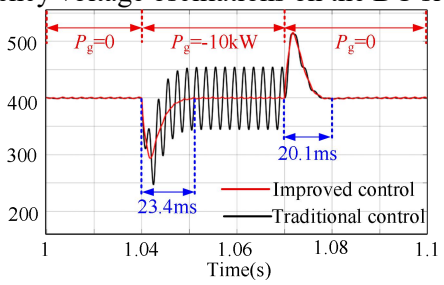


Figure 8. Grid-Side Power Step Test

5. Conclusion

This research systematically investigates the performance optimization of single-phase grid-connected inverter systems and proposes an improved DC bus voltage control method based on the conventional double-loop control architecture. Within this control framework, the current inner loop specifically employs a quasi-proportional resonant controller, whose strategic design aims to achieve precise and reliable reference signal tracking while effectively enhancing the system's overall stability margin and dynamic response performance. To address the inherent technical challenge of double-frequency ripple in the DC bus voltage commonly found in traditional control schemes, an innovative DC bus voltage extraction algorithm has been meticulously designed and implemented through advanced digital signal processing techniques. Comprehensive theoretical analysis and extensive experimental results demonstrate that the newly proposed algorithm offers dual advantages: it not only effectively suppresses the second-harmonic components present in the voltage outer loop but also enables the control system to achieve excellent dynamic response speed through

systematic parameter optimization. Furthermore, detailed simulation studies and rigorous experimental validation collectively indicate that the proposed control strategy consistently demonstrates excellent steady-state operating characteristics and outstanding dynamic performance metrics, thereby clearly confirming its technical correctness and engineering practicality in practical applications. Ultimately, the research findings and methodological contributions hold significant theoretical value and provide valuable engineering guidance for substantially enhancing the operational performance and reliability of single-phase grid-connected inverters in practical industrial applications.

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