A Literature Review on Low-Power Optimization of CMOS Temperature Sensors

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Abstract: With the rapid development of the Internet of Things and mobile devices, the demand for continuous accurate and low power consumption temperature monitoring has increased significantly. Therefore, CMOS temperature sensors have attracted wide attention because of their compatibility with IC technology, low cost and high integration. How to achieve low energy consumption under the premise of ensuring measurement performance has become a core design challenge. The strict power consumption requirements of application scenarios such as limited power supply, long-term standby and intermittent sampling have promoted the transformation of sensors to low power optimization. It has become a core issue to study how to achieve a compromise and balance between power consumption, accuracy, response speed and area.

CMOS temperature sensors have been widely used in portable electronic devices, Internet of things nodes, wearable terminals and on-chip thermal monitoring due to their compatibility with standard integrated circuit processes, low cost, small area, and easy integration with system-on-chip. In recent years, with the continuous development of edge intelligence and distributed sensing systems, low-power optimization has gradually become one of the core issues in the design of temperature sensing circuits. Focusing on the low power optimization problem of CMOS temperature sensor, this paper systematically expounds the collaborative optimization strategy of key modules such as temperature sensing front-end, signal processing circuit, analog-to-digital converter (ADC), digital filter and system architecture. In the thermal front-end, the exponential characteristics of sub-threshold MOSFETs are used to achieve nanoamperes static power consumption, and the dynamic biasing technology is combined to reduce the average power consumption. At the same time, how to maintain good linearity under very low bias current is analyzed. In the signal conditioning and ADC link, time domain technologies such as dynamic comparator and voltage to time conversion are used to replace the traditional high power consumption structure, and SAR or TDC architectures are optimized for different resolution requirements to realize the digitization of temperature signals with lower power consumption.

At the system level, this paper summarizes the top-level energy efficiency design schemes, such as periodic wake-up mechanism, fast start circuit, and one-bus digital interface, which reduce the average power consumption in standby and working states. Through literature research and comparative analysis, this paper sorts out the research results at home and abroad in the past two decades, constructs a technology evolution framework for CMOS temperature sensor low-power optimization, and quantitatively compares the power reduction effects of various methods. Research shows that multi-module collaborative optimization can break through the limitations of single circuit improvement, and provide energy-efficient and highly-integrated low-power optimization solutions for temperature sensors in application scenarios such as Internet of things, wearable devices and battery management systems.

Keywords: CMOS Temperature Sensor; Low Power Optimization; Subthreshold Technique; Dynamic Bias; System Architecture

1. Introduction

1.1 Research background and significance

With the continuous development of emerging applications such as Internet of things, mobile devices, smart healthcare and battery management systems, the energy efficiency of embedded sensor nodes is increasingly required.

Temperature is one of the most basic environmental and physiological parameters, and its sensing accuracy and power consumption level directly determine the endurance and use scheme of the whole system. CMOS temperature sensors have become the mainstream choice in the field of low-power sensing due to their high compatibility with standard integrated circuit technology, easy on-chip integration, and low cost. The temperature sensor market is expected to grow from $5.9 billion in 2021 to $8 billion by 2028, with a compound annual growth rate of 4.5% from 2021 to 2028 [1] In this context, how to reduce the static power consumption of temperature sensors to nanoamps and control the average power consumption below microwatts? It has become a key topic of common concern in academia and industry. Especially in the scenarios of edge computing and passive sensing, sensors are often in standby state for a long time and only wake up briefly when triggered by specific events, which poses higher challenges for system-level low-power architecture design.

Power management has always been one of the core issues in the design of temperature sensors. With the progress of CMOS technology, the integration degree continues to increase, but with it comes the aggravation of power consumption. The miniaturization and low power requirements of integrated circuits make the research of low power temperature sensors become the focus. [2] In recent years, the power consumption optimization of CMOS temperature sensors has shifted from single circuit improvement to multi-module cooperative evolution. Early research focuses on the physical characteristics of the temperature sensing element itself, such as using the base-emitter voltage (VBE) temperature coefficient of bipolar transistor (BJT) to achieve high-precision temperature measurement. However, the bias current is usually in the order of microamps, which is difficult to meet the energy consumption requirements of nanowatts. With the development of deep submicron and FinFET technology, the temperature sensing front-end based on the subthreshold region of MOSFET has gradually become a research hotspot. The leakage current of subthreshold MOSFETs varies exponentially with temperature, and theoretically it can achieve effective temperature sensing at tens of nanoamps bias, which is significantly better than the conventional BJT scheme. Xiao Linyang and others designed a temperature sensor based on the 0.13 μm CMOS process, which utilizes the ratio of subthreshold currents of NMOS transistors. This sensor adopts an architecture with two NMOS transistors of the same size, the same gate voltage, and different drain-source voltages. Under a 0.8 V power supply voltage, the overall power consumption is approximately 47.5 nW.[3]However, this technology path faces inherent defects such as poor linearity and process deviation sensitivity, which need to be improved by dynamic bias, digital calibration or feedback compensation, which constitutes the key contradiction of current low-power front-end design.

At the back end of the signal chain, the power consumption of analog-to-digital converters (ADCs) and filters has become increasingly prominent. Traditional high-precision Delta-Sigma ADCs have excellent noise shaping capabilities, but their continuous-time architecture relies on high-gain operational amplifiers, which makes it difficult to compress the static power consumption. In contrast, Successive Approximation (SAR) ADCs and time-to-digital converters (TDC) show significant energy efficiency advantages in low sampling rate scenarios by virtue of the switched capacitor structure and time-domain processing mechanism. For example, a TDC-based CMOS temperature sensor reported at ISSCC 2022 achieves 0.1°C resolution at 1 SPS sampling rate and consumes only 0.8 μW overall. At the same time, the low-frequency 1/f noise becomes the main bottleneck limiting the SNR at the nanoamp level bias. Chopper Stabilization technology can shift the low frequency noise to high frequency through modulation and demodulation, and then suppress the noise efficiently with switched capacitor filter. It can increase the Effective number of bits (ENOB) without introducing high-power op-amp.

From the perspective of system architecture, it is difficult to optimize the energy consumption of only one part to meet the complex needs of the market, and the top-level power management strategy must be introduced. By setting a fixed or adaptive time interval to activate the sensor and maintaining a deep sleep state for the rest of the time, the periodic wake-up mechanism can reduce the average power consumption by more than two orders of magnitude. With the Fast Wake-up Circuit, the system can complete the temperature acquisition and data output in

hundreds of microseconds, avoiding the waste of energy caused by long warm-up. In addition, the single-bus digital interface only needs one data line to complete power supply and communication, which simplifies wiring and further reduces the power consumption of peripheral circuits. Yole Developpement, a market research firm, pointed out that about 35% of the global smart wearable devices in 2023 use integrated CMOS temperature sensors, and more than half of them have deployed periodic wake-up and fast start technology. In summary, the low-power optimization of CMOS temperature sensors has entered a new stage of "device - circuit - system" three-level collaboration.

1.2 Research Purpose

With the rapid development of emerging applications such as Internet of things, wearable devices and smart battery management systems, embedded temperature sensor nodes are required to achieve both extreme low power consumption and high integration. According to IDC data, global wearable device shipments have reached 539 million units in 2023, and are expected to exceed 800 million units in 2027. According to a Statista report, the number of iot connected devices worldwide has exceeded 14.4 billion in 2022 and is expected to reach 27 billion in 2025. In this context, as the key sensing unit, the power consumption level of CMOS temperature sensor directly restricts the endurance and deployment density of the whole system. Most traditional temperature sensors use bipolar transistor (BJT) as the temperature sensing element, which has good accuracy, but it is difficult to be fully compatible with standard CMOS process, and the static power consumption is generally in the order of microamps, which is difficult to meet the needs of nanowatt to microwatt level energy constrained scenarios. Therefore, it is necessary to systematically explore the collaborative optimization path from device physical characteristics to system-level energy efficiency management around the full CMOS compatible architecture, so as to realize the unification of nanoan-level static power and high linearity, and provide the core support for the next generation of ultra-low power sensing systems.

This paper aims to construct a complete low-power technical framework covering front-end temperature sensing, signal conditioning, analog to digital conversion, noise suppression and system architecture by deeply analyzing the power consumption composition and optimization potential of each functional module of CMOS temperature sensor. In the temperature sensing circuit, we focus on how to use the inherent exponential temperature characteristics of MOSFETs in the subthreshold region to achieve high sensitivity under nanoampere-level bias current, and avoid continuous static power consumption through dynamic bias strategy. In the signal processing, the traditional high-power operational amplifier is abandoned, and the switched capacitor structure and chopper stabilization technology are adopted to suppress 1/f noise. In the digitization stage, SAR or Time-to-Digital Converter (TDC) architecture was reasonably selected according to the different resolution and delay requirements of application scenarios, and dynamic comparator and time-domain signal processing method were introduced to eliminate static power consumption. At the system level, the periodic wake-up mechanism, fast start circuit and single bus interface protocol are integrated to significantly reduce the standby energy consumption and shorten the effective working time. Through the systematic sorting and quantitative comparison of research results at home and abroad in the past two decades, this study not only lists the applicable boundaries and energy efficiency gains of various optimization techniques, but also reveals the breakthrough effect of multi-module collaborative design on the overall power consumption bottleneck. Therefore, it provides theoretical basis and technical route guidance for energy-efficient temperature sensing solutions in the fields of Internet of things terminals, implantable medical devices and wireless sensor networks.

1.3 Research status at home and abroad

In recent years, with the rapid development of the Internet of things, wearable devices and wireless sensor networks, the demand for low-power CMOS temperature sensors is increasing. Internationally, researchers generally focus on reducing power consumption through circuit architecture innovation and process optimization. For example, the MOS transistor design with subthreshold workspace, the introduction of time domain or frequency domain signal conversion mechanisms, and the

use of on-chip calibration techniques to reduce energy consumption due to external intervention are used. These methods significantly improve the energy efficiency, so that the sensor still has high accuracy under microwatt or even nanowatt power consumption. At the same time, domestic research has also made positive progress, especially in the integrated low power design for specific application scenarios (such as passive RFID systems). In his paper, Huan Zhang improved and optimized the design of passive UHF RFID tag chip, and the low power consumption strategy involved in it has important reference significance for the design of CMOS temperature sensor. The research points out that the power consumption of the chip can be reduced as much as possible by enabling the control signal to control the power off of some modules to reduce unnecessary power consumption. For example, the modulation and demodulation modules are turned on when needed and turned off when unnecessary, which effectively reduces the overall chip power consumption and provides a feasible path for the power control of the embedded temperature sensor unit. Although many achievements have been made in the field of low-power CMOS temperature sensors at home and abroad, there are still challenges in balancing high precision, wide temperature measurement range and low power consumption, which need further exploration and research. [4]

In China, many scholars have carried out in-depth exploration around different application scenarios. Lei Bincheng designed a BJT-based low-power temperature sensor for low-voltage power supply environment, and integrated a 10-bit SAR ADC to achieve low power consumption while ensuring temperature measurement accuracy. [2] Xiao also focused on low-voltage and low-power design, generating PTAT relationship based on subthreshold current ratio, and using current-frequency conversion circuit to realize the conversion of temperature to digital signal. [3] Yu Xianyin proposed a temperature sensing circuit based on subthreshold MOSFET. The circuit structure is simple, and the average current of the temperature sensing module is only 76.48nA, which is suitable for general embedded systems. [5] Xinyu Zhao focused on power consumption optimization of digital modules and proposed a low-power digital filtering architecture, which could adjust the number of operation units according to the difference between the measured temperature and the threshold interval. [6] Yiqiang Zhao et al. further optimized the digital signal processing link and achieved 20.15μW power consumption of digital module in 180 nm CMOS process. [7] From the perspective of high precision, Qian Fuyue designed an all digital temperature sensor based on frequency domain and a voltage domain temperature sensor based on BJT, and reduced the error through curvature compensation and chopping zero stability technology. [8] From the perspective of a wide temperature range, Yang Luhan adopted a RC oscillator structure based on frequency-locked loop, and achieved a 3σ measurement accuracy of ±1.0℃/0.8℃ in the range of -40℃ to 125℃. [9] Hua Wenho conducted a high-precision integration scheme to verify the applicability of the parasitic BJT structure in modern CMOS process. [1]

In terms of application integration, Hou Lujin et al. embedded a low-power CMOS temperature sensor integrated with UHF RFID into an ultra-high frequency radio frequency identification tag, and the final temperature sensing error was relatively small. [10] Liu Haoyu developed a low-power temperature sensor for MEMS clock system temperature compensation, achieving temperature-to-frequency conversion through an RC oscillator, thus avoiding the high power consumption bottleneck brought by traditional ADCs. [11] Shen Bing also designed a temperature-sensing front-end based on subthreshold amplifiers for temperature-compensated crystal oscillators, significantly reducing the overall system energy consumption. [12] Li Yujia et al. conducted early research on integrating temperature sensors in ASICs for MEMS devices, laying the foundation for subsequent on-chip system thermal management. [13] Fan Xudong designed an on-chip temperature sensor based on an RC oscillator structure, using a lookup table method to convert counter values to temperature, expanding the application of CMOS temperature sensors in SD/MMC controllers. [14] Tang Zhong proposed multiple novel architectures such as a capacitor-reuse type voltage-to-duty cycle converter from a low-cost implementation perspective, expanding the application boundaries of CMOS temperature sensors in consumer electronics. [15] Domestic research has formed a complete technical chain covering

process adaptation, circuit architecture, digital back-end, and system integration, and has achieved many low-power optimizations.

1.4 Research Content

This study focuses on the key technology path of low-power optimization of CMOS temperature sensors, and systematically conducts collaborative optimization analysis around five core modules: temperature sensing front-end, signal processing circuit, analog-to-digital converter (ADC), filter and overall system architecture. In the thermal front-end, the exponential temperature characteristics of the MOSFET based on the subthreshold region are studied, and the operating current is reduced to nanoamperage to achieve low power optimization. Combined with the dynamic biasing technology, the average power consumption is significantly reduced by turning off or reducing the bias current during the non-sampling period. At the same time, for the problem of linearity deterioration under very low bias conditions, the compensation algorithm and structure improvement strategy are studied to ensure that the temperature response can still maintain high precision under weak current. In the signal conditioning process, the focus is on how to complete the amplification and preprocessing of weak analog signals with minimum energy consumption, avoiding the power burden caused by traditional high-gain op-amp, and switching capacitors or time-domain comparison structures are used to achieve efficient signal conversion. At the ADC design level, the energy efficiency performance of SAR ADC and TDC (time-to-digital converter) architecture is compared according to different application scenarios, and the time domain technologies without static power consumption, such as dynamic comparator and voltage to time conversion, are preferred to complete the digitization process of temperature signal with the lowest energy cost.

In the aspect of noise suppression, the chopper stabilization technology and the switched capacitor filter are co-designed to effectively suppress the inherent 1/f low-frequency noise of CMOS process without relying on the high-power operational amplifier, so as to improve the signal-to-noise ratio and long-term stability. At the system architecture level, the periodic wake-up mechanism is introduced from the top level of energy efficiency, so that the sensor is in a deep sleep state most of the time, and only starts and completes the measurement at the scheduled sampling time, which greatly reduces the standby power consumption. At the same time, the single-bus digital interface protocol was optimized to reduce the communication overhead and the number of pins, further compressing the overall energy consumption of the system. In terms of research methods, literature research and comparative analysis were comprehensively used to retrieve core literature of Google Scholar and CNKI in the past two decades, and the time line of technology evolution of each module was constructed. Some specific cases, such as parasitic diode temperature sensing, Delta-Sigma and SAR ADC energy efficiency comparison, CIC/FIR filter low power implementation under FinFET process are analyzed.

2. Theoretical Basis and Technical Framework for Low Power Optimization of CMOS Temperature sensor

2.1Basic principle and classification of CMOS temperature sensing

As an indispensable sensing unit in modern integrated circuits, the basic working principle of CMOS temperature sensor depends on the characteristics of physical parameters such as carrier mobility, threshold voltage or junction voltage in semiconductor materials as a function of temperature. CMOS temperature sensor is mainly divided into two categories based on bipolar transistor type (BJT) and MOSFET type. BJT type sensor uses the relationship between base-emitter voltage VBE and temperature in inverse or direct proportion to construct a temperature sensitive circuit, which has high accuracy and good linearity, typical representative such as Brokaw bandgap reference structure. On the other hand, the MOSFET scheme is more dependent on the threshold voltage VTH or the exponential response of leakage current in subthreshold region to temperature. Especially in advanced CMOS process nodes, due to the limited performance of parasitic BJT, MOSFET scheme is gradually becoming the mainstream because of its full CMOS compatibility and high integration advantage. In recent years, with the increasing power consumption requirements of the Internet of Things and wearable devices, the temperature sensing front-end based on FinFET

or FD-SOI has been widely explored, which further expands the technical boundaries of CMOS temperature sensing.

CMOS temperature sensor can also be divided into analog output type and digital output type according to the output form. Analog type usually directly output voltage or current signal proportional to the temperature, the structure is simple but susceptible to the interference of circuit noise after stage. The digital type has a built-in analog-to-digital converter and outputs digital temperature values through I²C, SPI or single bus interfaces, which has stronger anti-interference ability and system integration convenience.

It can also be divided into continuous working type and intermittent wake-up type according to power consumption level. The continuous operation type is suitable for high real-time scenarios, but the static power consumption is high. The intermittent wake-up mode reduces the average power consumption to microwatt or even nanowatt level under the premise of guaranteeing functionality through periodic sleep and fast start mechanism.

In terms of chip area and power consumption, the full MOSFET temperature sensor has significant advantages in ultra-low power consumption and small area, but its linearity and accuracy are relatively low. However, BJT has higher accuracy although it has higher power consumption. With the introduction of dynamic bias and calibration algorithms, the performance gap of MOSFET-type sensors is narrowing, especially in 28 nm and below processes, where the area efficiency and cost advantages make them dominant in consumer electronics. This technology evolution trend indicates that low-power optimization has shifted from single device selection to a new stage of multi-module co-design. [15]

2.2 Power consumption composition and key technologies

The power consumption of CMOS temperature sensor can be analyzed from two dimensions: static power consumption and dynamic power consumption. Static power consumption is mainly caused by leakage current and bias current in the non-switching state of the circuit, which is especially dominant in the thermal front-end and analog signal chain. In traditional BJT-based bandgap reference structures, hundreds of microamps of bias currents are usually required to maintain good linearity and temperature sensitivity, resulting in high static power consumption. The MOSFET temperature sensing unit operating in the subthreshold region can reduce the quiescent current to nanoamp level, but it is more sensitive to process variation and power fluctuations, and it is easy to introduce nonlinear errors at very low bias. Dynamic power consumption is mainly generated by analog-to-digital converter and digital interface and periodic wake-up, and is proportional to the working frequency, load capacitance and the square of supply voltage. In intermittent work scenarios such as iot terminals, although sensors are in standby mode most of the time, frequent wake-up and sampling processes still cause energy consumption. It has been reported in literature that the analog front-end (including temperature sensing circuit and bias) is the main source of energy consumption in a typical CMOS temperature sensor. Therefore, the key bottleneck of power optimization is how to compress the static and dynamic power while maintaining the accuracy and response speed. In particular, it is necessary to solve the problems such as sub-threshold front-end linearity deterioration, low ADC conversion energy efficiency, and system-level standby power consumption.

Further analysis shows that the power consumption bottleneck of current CMOS temperature sensors presents the module coupling characteristics, and the optimization of a single module is often limited by the constraints of upstream and downstream circuits. For example, reducing the bias current of the temperature sensing front-end can reduce the static power consumption, but it will weaken the signal-to-noise ratio, forcing the subsequent amplifier or ADC to improve the gain or resolution, which will increase the overall energy consumption. In addition, 1/f noise significantly affects the long-term stability of DC-coupled systems at low frequency bands. Traditional schemes rely on high-gain op-amp with chopper technology to suppress noise, but the op-amp itself consumes high power. Recent industry data show that with the increasingly stringent energy efficiency requirements of wearable devices and wireless sensor nodes, academia and industry have accelerated the promotion of collaborative optimization strategies. TMP117, a high-precision, low-power CMOS temperature sensor chip introduced by TI

in 2018, can measure temperature from -55°C to 150°C with a maximum temperature error of ±0.3°C and can operate in a wide power supply range of 1.8V to 5.5V with a typical current of only 3.5μA.

2.3 Core index system of low-power design

The core indicators of low-power design are to evaluate the energy efficiency performance of CMOS temperature sensors. Their construction needs to take into account multiple factors such as static and dynamic power consumption, accuracy, response speed, and system integration. In the current rapid development of the Internet of Things and mobile devices, the global low-power sensor market is continuously expanding. Under this trend, static low-power optimization has become an important indicator, especially in long standby scenarios, if the temperature sensing front-end adopts the sub-threshold MOSFET structure, its static current can be as low as several hundred picas to several nanos, significantly superior to the traditional BJT solution. At the same time, average power consumption is also very important. It is determined by the working cycle, wake-up frequency, and transient power consumption, and is usually optimized through a cycle wake-up mechanism and a fast start-up circuit to make the sensor remain in deep sleep for more than 99% of the time, thereby controlling the annual average energy consumption at an extremely low level. In addition, energy efficiency, as a key parameter for measuring the overall energy efficiency of ADC and signal chain, has achieved a level of less than 1 pJ/sample in advanced literature in recent years.

Apart from power consumption indicators, accuracy and linearity also constitute inseparable constraints for low-power design. The measurement accuracy requirement for medical wearable temperature sensors is generally ±0.1°C to ±0.5°C, while industrial battery management systems (BMS) generally accept an error range of ±1°C. However, under extremely low bias current, the signal-to-noise ratio of the temperature sensing element decreases, which can easily lead to an increase in non-linear errors. Therefore, dynamic bias or digital calibration techniques must be introduced to maintain linearity. In terms of noise performance, 1/f noise dominates in the low-frequency range, especially more significant in the sub-threshold working area. Therefore, the effective noise bandwidth (ENBW) and equivalent input noise (RTI Noise) become important bases for filter design. In recent years, filters combining chopping stabilization and switch capacitor technology can suppress noise to below 10 μVrms without using high-power amplifiers, meeting the requirements of high-resolution temperature sensing. In summary, the indicator system of low-power CMOS temperature sensors has shifted from solely pursuing low current to a multi-objective collaborative optimization paradigm of "power - performance - area" (PPA).

2.4 Division of Technical Paths and Logical Logic of Synergistic Optimization

The low-power optimization of CMOS temperature sensors can be divided into three technical paths: device level, circuit level, and system level. At the device level, the core lies in leveraging the exponential current-temperature characteristic of MOSFETs in the sub-threshold region of the CMOS process to achieve a nanometer-level static power consumption for the temperature sensing front-end. Over the past five years, with the widespread adoption of advanced process nodes such as 28 nm and below, the FinFET structure has significantly improved the sub-threshold slope, enabling the temperature sensing sensitivity to remain at a high level even under extremely low bias currents. At the same time, dynamic biasing technology has been widely introduced, compressing the average power consumption to the picowatt level by activating the temperature sensing unit only during the sampling period. However, this path faces challenges such as degradation in linearity and sensitivity to process variations, which require compensation through calibration algorithms or differential structures. At the circuit level, signal conditioning and analog-to-digital conversion become the key to power optimization. Traditional high-gain operational amplifiers have gradually been replaced by dynamic comparators and time-domain processing techniques such as voltage-time conversion (VTC), especially in IoT nodes with demands for low to medium resolution (8–12 bits). Successive approximation (SAR) ADCs have become the mainstream choice due to their simple structure and linear power consumption with respect to sampling rate, while time digital converters (TDCs)

demonstrate higher energy efficiency in ultra-low power scenarios. For instance, a temperature sensor architecture with a TDC design developed by researchers at Southeast University in 0.18 μm CMOS process achieved ±0.1℃ accuracy while consuming only 3.8 μW. [16] Additionally, to suppress the inherent 1/f noise of CMOS processes, the design of chopping stabilization technology and switch capacitor filters has become an important direction. By periodically modulating the signal spectrum to avoid the low-frequency noise region and avoiding the use of high-power continuous-time amplifiers, noise performance and energy efficiency can be balanced.

System-level optimization focuses on overall working modes and interface design, emphasizing on-demand power supply and rapid response coordination logic. The periodic wake-up mechanism is the current mainstream solution. The sensor is mostly in a deep sleep state, only being briefly awakened by low-power real-time clocks or external events, and quickly returning to sleep after completing the measurement. Combined with a fast-start circuit, the effective working time can be compressed to the microsecond level, significantly reducing power consumption. The ultimate optimization of a single module is often limited by the overall energy efficiency bottleneck of the system, and only through cross-level collaboration can the maximum energy-saving potential be released. For example, the dynamic range of the temperature sensing front-end output signal directly affects the quantization accuracy and power consumption of the ADC, while the conversion speed of the ADC determines the system's wake-up duration. Therefore, the research trend in recent years has shifted from single optimization to end-to-end joint design: embedding the non-linear characteristics of the temperature sensing unit into the ADC encoding strategy, or using digital domain calibration instead of high-power consumption compensation circuits in the analog domain. This collaborative logic not only aligns with the integration advantages brought by the continuous miniaturization of CMOS processes but also conforms to the comprehensive requirements of IoT terminals for high energy efficiency, small area, and low cost. According to market research institution Statista, based on reports from institutions such as Mordor Intelligence, the global temperature sensor market size is approximately $9.35 billion in 2025 and is expected to reach $12.68 billion in 2030, with a CAGR of approximately 6.28%. This highlights the broad application prospects of this technology path in smart wearables, industrial monitoring, and battery management of new energy vehicles.

3. Low-power Optimization Methods for Temperature-sensing Front-end and Signal Processing Circuits

3.1 Temperature Sensing Mechanism based on the Sub-threshold Region of MOSFET

3.1.1 Modeling of exponential characteristics in the sub-threshold region and temperature sensitivity

In the CMOS process, when MOSFET operates in the sub-threshold region, its drain current is in an exponential relationship with the gate-source voltage.Since VT is linearly proportional to temperature, and the VTH (threshold voltage) in the exponential term usually has a negative temperature coefficient (approximately -2 mV/°C), by reasonably configuring multiple MOSFETs to form a differential or proportional structure, a strong temperature-related output signal can be extracted. In recent years, with the continuous improvement of energy efficiency requirements for IoT terminals, temperature sensing circuits based on sub-threshold MOSFETs have also become a research hotspot. In CMOS process nodes ranging from 0.18 μm to 55 nm, the design of low-power temperature sensors using sub-threshold MOSFETs as the temperature sensing front-end has become the mainstream trend. Their static current can generally be controlled at the microampere or even nanometer level. For example, scholar Yu Xianyin designed a temperature sensing module based on 130 nm CMOS process, with a design simulation conducted under a power supply voltage of 0.6V, and the temperature variation range was relatively small, from 17°C to 59°C. The average current of the temperature sensing module was 76.48 nA.

The theoretical upper limit of temperature sensitivity is limited by the ratio of the sub-threshold slope to the thermal voltage. In practical applications, the effects of process angle variations, power supply fluctuations, and parasitic effects need to be considered. In traditional planar CMOS processes, the sub-threshold slope factor n is usually in the

range of 1.3 to 1.7. In recent years, through circuit structure optimization, the performance of sub-threshold temperature sensors can be significantly improved without relying on advanced processes. For example, Yu Xianyin from University of Electronic Science and Technology of China designed a low-power CMOS temperature sensor in 2021, using MOSFETs operating in the sub-threshold region as the temperature sensing element. At an ultra-low power supply voltage of 0.6V, the average current of the temperature sensing module was only 76.48 nA. Through optimization design within the temperature range of 35°C to 42°C for human body temperature measurement, this sensor achieved high accuracy of ±0.1°C. Its temperature sensing circuit adopts a differential structure, generating a positive temperature coefficient voltage through the cascading of 7 differential units, effectively eliminating the temperature dependence of the threshold voltage Vth on the accuracy. [6]

Furthermore, industry data indicates that there has been a significant increase in the demand for nano-watt level sensors in the global wearable device market. Therefore, establishing a comprehensive sensitivity model that includes process parameters, temperature range, and power consumption constraints has become a core prerequisite for the design of low-power CMOS temperature sensors. This model not only guides the selection of devices and the setting of bias points, but also provides a theoretical basis for subsequent linearity compensation and system collaborative optimization.

3.1.2 Linearization compensation strategy under nanometer-level bias current

Under the Nanchan bias current condition, although the exponential characteristics of the sub-threshold region of MOSFETs are beneficial for reducing power consumption, they result in a non-linear relationship between the output signal and temperature, severely restricting the measurement accuracy of the sensor in a wide temperature range. The typical non-linear error can reach more than ±5°C, making it difficult to meet the requirements of industrial or medical applications. Therefore, researchers have proposed various linearization compensation strategies, with the core strategy being to counteract the high-order influence of the exponential term through circuit topology reconfiguration or signal post-processing. Early methods often used resistor networks or diode strings for analog domain correction, but this would introduce additional power consumption and area overhead. In recent years, mainstream solutions have shifted to designs based on proportional current or voltage differential structures. For example, by using two MOSFETs of the same size but with different biases to form a current mirror, the logarithmic form of the current ratio can approximately linearize the temperature response. In the design of CMOS temperature sensors, Xiao Linyang from University of Electronic Science and Technology of China proposed in 2022 a low-power temperature sensing circuit based on the sub-threshold current ratio, using two identical NMOS transistors, applying different source-drain voltages to make them operate in the sub-threshold region. At a 0.8V power supply voltage, the temperature sensing unit achieved a linear error of +0.23°C / -0.24°C within the temperature range of 0°C to 80°C. The static current of the temperature sensing unit was only at the nanometer level, and the overall temperature sensor was fabricated in a 0.13μm CMOS process, with a total power consumption as low as 47.5nW. The key to this method lies in precisely matching device parameters and suppressing the secondary non-linearity caused by process mismatches. [3] Another effective strategy is to combine digital domain calibration with on-chip storage technology. With the miniaturization of CMOS processes, the cost of on-chip EEPROM or OTP memory has significantly decreased, enabling the calibration coefficients to be embedded in the chip. Industry data shows that from 2020 to 2024, the proportion of CMOS temperature sensors using digital compensation increased from 31% to 58%, reflecting the advantage of this path in the feasibility of mass production. Additionally, dynamic biasing technology is also used to improve transient linearity. During the sampling period, the bias current is temporarily increased to accelerate the establishment, and then returns to the nanometer level to maintain the state, ensuring response speed without excessively increasing power consumption.

3.2 Dynamic Bias Technology

The bipolar transistor (BJT) is a widely integrated temperature sensing element in CMOS technology. Its base-emitter voltage VBE has a clear negative temperature coefficient

characteristic of approximately -2 mV/°C, which stems from the exponential relationship of the intrinsic carrier concentration of semiconductor materials with temperature. In traditional CMOS temperature sensors, the difference in VBE under two different collector current biases, ΔVBE, is often used as the temperature sensing signal, as its positive temperature coefficient characteristic (approximately +85 μV/°C) is more conducive to subsequent linearization processing. However, to achieve the goal of low power consumption, the bias current must be reduced to nanohm or even picohen range, which can significantly reduce the static power consumption to below 100 nW, but will introduce severe thermal noise and shot noise, and also result in an excessively small ΔVBE amplitude, making it difficult for subsequent circuits to effectively amplify. In recent years, scholars have optimized the current ratio, introduced pulse width modulation, and adopted high gain low offset operational transconductance amplifiers (OTA) to suppress the noise impact while maintaining the detection capability of weak signals. Zhejiang University's Tang Zhongyu designed a BJT temperature sensor based on 55 nm CMOS technology, using dynamic current gain compensation technology. Without increasing additional power consumption, area, etc., it effectively suppressed the influence of the limited current gain ($\beta < 1$) of the PNP transistor on the accuracy of VBE under advanced process technology. The sensor adopts a current domain readout architecture and a first-order continuous-time DeltaSigma modulator. At a 2.5V power supply voltage and a 1 MHz system clock, the total bias current is only 37 μA. Through dynamic element matching (DEM) and chopping techniques to eliminate device mismatch and low-frequency noise, the sensor achieves a ±1.7°C (3σ) uncalibrated accuracy within a wide temperature range of -40°C to 125°C, with a core area of only 0.0146 mm². Although the BJT temperature sensing front-end has good theoretical linearity and mature design methods, it is sensitive to process variations, especially in advanced CMOS nodes, where parasitic effects increase, leading to intensified VBE drift, limiting its long-term stability in ultra-low power consumption scenarios.

To address these challenges, dynamic biasing technology has become a key breakthrough. This strategy shuts off the BJT bias current during non-sampling periods and only turns it on during measurement, compressing the average power consumption to the nanowatt level. Combined with a fast startup circuit, it can complete bias establishment and signal acquisition within a few microseconds, avoiding the accumulation of long-term static power consumption. Additionally, BJT can be integrated with MOS devices, using MOS transistors to construct current mirrors instead of traditional resistive loads, further reducing the voltage margin requirements and adapting to power supply environments of 1 V or below. According to industry data from 2020 to 2024, the proportion of CMOS temperature sensors with BJT front-ends in global IoT devices still reaches 42%, mainly used in smart meters, industrial monitoring, and other scenarios with high precision requirements and allowable microampere-level power consumption. However, in the nanowatt energy efficiency requirements of wearable devices and other fields, BJT is gradually facing the trend of being replaced by new MOS-based temperature sensing structures due to its limited minimum operating current being limited by the physical limits of bipolar devices. Therefore, how to balance noise performance, linearity, and process robustness while operating at extremely low bias conditions remains the core issue for optimizing the low power consumption of the BJT temperature sensing front-end.

3.3 Dynamic Biasing and Adaptive Power Supply Technology

3.3.1 *Dynamic bias current control principle and circuit implementatio*n

Dynamic bias current control is one of the key technologies for achieving low power consumption in CMOS temperature sensors. Its core idea lies in dynamically adjusting the bias current of the temperature sensing front end based on the sensor's operating state, ensuring low power consumption while maintaining measurement accuracy. The traditional static bias scheme requires a constant bias current to maintain continuous operation, which consumes energy continuously during non-sampling periods and is difficult to meet the requirements of nano-ampere-level standby power consumption for IoT nodes and other devices. On the other hand, dynamic bias introduces timing control logic to briefly activate a high bias current during the sampling period to ensure

signal quality, while reducing the bias to sub-threshold or even turning it off during the rest of the time, thereby compressing the static power consumption to an extremely low level. This technology is usually implemented by combining a digital control unit with an analog switch circuit, for example, using MOS switches to control the gate voltage or source-drain path of the temperature sensing transistor, and combining it with a low-power oscillator to generate precise enable pulses. In recent years, research based on CMOS processes of 65 nm and below has shown that dynamic bias can reduce the average current of the temperature sensing front end from micro-ampere level to tens of nanohenries, while maintaining a temperature measurement error of ±0.5°C.

In terms of circuit design, dynamic bias is often designed in conjunction with sub-threshold MOSFET temperature sensing structures. Due to the exponential relationship between the leakage current of sub-threshold MOSFETs and temperature, they inherently have high sensitivity, but their output signals are weak and susceptible to process variations. Dynamic bias increases the signal-to-noise ratio and accelerates circuit setup by injecting sufficient bias current at the sampling instant, then quickly returning to the sub-threshold state to reduce power consumption. Typical implementations include using charge pumps or capacitor energy storage units to provide transient current during the enable period to avoid additional losses caused by directly relying on power rails. Additionally, a feedback mechanism can be introduced to adaptively adjust the bias pulse width or amplitude based on the environmental temperature to cope with the non-linear changes in device characteristics in different temperature ranges.

3.3.2 Trade-off mechanism between energy efficiency and response speed

In the low-power optimization of CMOS temperature sensors, there is an inherent trade-off between energy efficiency and response speed. This contradiction mainly stems from the influence of dynamic bias and sub-threshold operation on the circuit setup time. When the bias current is significantly reduced to achieve the ultimate energy efficiency, the time constants of the temperature sensing front-end and the subsequent signal conditioning circuits increase significantly, resulting in an extended time required for the system to transition from sleep to stable output, thereby limiting the maximum effective sampling rate. For example, at the nanohenry bias level, the transconductance of the MOSFET drops sharply, and the unit gain bandwidth of the amplifier may be less than 1 kHz, making a single temperature conversion take several hundred milliseconds to complete, which cannot meet the requirements of rapid temperature monitoring scenarios. Therefore, how to achieve acceptable response performance within a limited energy budget has become a key challenge in the application of dynamic bias technology. Recent research has generally adopted the "fast start slow measurement" strategy, that is, applying a brief high-current pulse at the beginning of the wake-up to accelerate circuit setup, and then switching to a low-bias mode for precise sampling, thereby shortening the effective response time while keeping the overall energy consumption controllable.

3.4 Design of Low-Power Signal Conditioning Circuit

In CMOS temperature sensors, the voltage signal output by the temperature sensing front-end is usually at the millivolt level and is susceptible to process variations and environmental interference. Therefore, it must be amplified through a low-noise, high-gain signal conditioning circuit. However, although traditional operational amplifiers can achieve nanohenry-level static current in the sub-threshold or near-threshold operating region, they have difficulty overcoming the 1/f noise problem caused by the inherent characteristics of MOSFETs, especially showing significant degradation in signal-to-noise ratio at low frequencies, thereby affecting the temperature measurement accuracy. To address this challenge, chopper stabilization (Chopper Stabilization) technology has been widely introduced into the design of weak signal amplifiers. This technology modulates the original signal at a high frequency at the input end, moving it to a frequency band away from the 1/f noise dominance, and then amplifies and demodulates it back to the baseband, effectively suppressing low-frequency noise. In recent years, with the increasing requirements for energy efficiency in the Internet of Things and wearable devices, the selection of chopper frequency and power consumption control have become research hotspots. However, the chopper operation itself

introduces switch charge injection and clock feedback errors, and if not resolved, it may introduce new nonlinear distortions. Therefore, modern low-power chopper amplifiers often combine self-stabilized zero or dynamic component matching techniques for compensation to balance noise suppression and linearity.

Furthermore, in response to the dual constraints of area and power consumption on CMOS temperature sensors, researchers are dedicated to simplifying the chopper architecture and reducing its additional overhead. The traditional dual-phase chopper structure requires two sets of complementary clocks and multiple levels of switch networks, which not only increase the layout area but also cause an increase in dynamic power consumption due to frequent switching operations. Therefore, the single-phase chopper and asynchronous chopper schemes that emerged after 2020 have significantly improved energy efficiency performance.

4. Collaborative Low-Power Design of ADC, Digital Filtering and System Architecture

4.1 Analog-to-Digital Converter

4.1.1 Energy efficiency advantage of SAR ADC in medium-resolution scenarios

The successive approximation register type analog-to-digital converter (SAR ADC) has gradually become the mainstream choice for the digitalization process of CMOS temperature sensors due to its simple structure, controllable power consumption, and high energy efficiency ratio at medium resolutions. In the context of IoT and wearable devices where power consumption is extremely sensitive, SAR ADC outperforms continuous operation pipelines and DeltaSigma architectures due to its on-demand operation characteristic. This advantage stems from its core modules, the capacitor array DAC and the dynamic comparator, which consume energy only during sampling and comparison, and remain in a sleep state during the rest of the time. Especially in low-frequency signal processing scenarios such as temperature sensing, the intermittent operation mode of SAR ADC and the system's periodic wake-up mechanism are highly compatible, avoiding unnecessary static current loss. Moreover, through the adoption of segmented capacitor arrays, self-boost switches, and low swing clock technologies in recent years, the switching noise and dynamic power consumption have been further suppressed, enabling a 12-bit SAR ADC to maintain sub-micro watt-level power consumption at a 180 nm process, meeting the dual requirements of industrial-grade temperature monitoring for accuracy and energy efficiency.

SAR ADC demonstrates the optimal energy-precision trade-off in the medium resolution (8–12 bits) range. Compared with the data of more than ten ADC chips for temperature sensing published from 2020 to 2023, the SAR architecture has an average power consumption of only 1/5 to 1/3 of Delta-Sigma ADC at 10-bit accuracy, and the area overhead is reduced by approximately 40%. Lei Bincheng's 10-bit SAR ADC, also used for temperature sensors, achieves a low power consumption of 9.54 nW under a 0.6 V power supply through the optimization of the logic timing control structure, demonstrating the great potential of the SAR architecture in low-power temperature measurement applications. The key to this energy efficiency advantage lies in its elimination of high-gain operational amplifiers and complex digital filters, significantly reducing the static bias current in the analog front end. Meanwhile, as the process node shrinks to 28 nm and below, the threshold voltage of MOS transistors decreases, allowing the dynamic comparator to operate reliably at lower power supply voltages (such as 0.6 V), further compressing power consumption. Therefore, in temperature sensing applications with moderate resolution requirements but extremely sensitive to battery life, SAR ADC has become the preferred architecture that balances performance and energy efficiency. Its optimization space still focuses on capacitance matching error correction and low-power timing control strategies. [2]

4.1.2 The mechanism of TDC and time domain conversion technology in eliminating static power consumption

The Time-Digital Converter (TDC) and time-domain signal processing technology provide an innovative path for CMOS temperature sensors to completely avoid static power consumption. Traditional voltage-domain ADCs rely on continuous biasing operational amplifiers or comparators, which have non-negligible leakage current even in idle states; while the TDC encodes temperature information as time intervals (such as pulse width or

oscillation period), activating logic gate circuits only at the moment of signal conversion and completely turning off during the rest of the time, thus achieving extremely low static power consumption. This mechanism is applicable to CMOS temperature sensing front-ends based on ring oscillators or delay chains, where temperature changes directly modulate the oscillation frequency or propagation delay, and the output signal naturally represents the temperature in time form.

The low power consumption of TDC stems from its fully digital or quasi-digital implementation method. In recent years, researchers have introduced asynchronous TDC, cursor delay lines, and time amplification techniques to significantly reduce active energy consumption while maintaining medium accuracy (±0.5°C). Moreover, the high integration of TDC with the temperature sensing front-end also reduces the signal conditioning 环节， eliminating the necessary transimpedance amplifiers or buffers in traditional solutions. Industry data shows that the proportion of low-power CMOS temperature sensors published between 2019 and 2023 has increased from 12% to 37%， reflecting its increasing presence in nanowatt-level application scenarios. Although TDC is sensitive to process variations and power supply noise， it can achieve reliable operation through on-chip calibration and differential structure design. Therefore， TDC not only eliminates the static power consumption bottleneck but also promotes the leap in system-level energy efficiency through simplified architecture.

4.1.3 The balance between high precision and power consumption of DeltaSigma ADC

The Delta-Sigma ADC, with its built-in noise shaping and high-resolution capabilities, remains indispensable in CMOS temperature sensing applications that require ±0.1°C or higher precision. However, its high oversampling rate and complex digital filters come with significant power consumption costs. Traditional first-order or second-order modulators can alleviate power consumption pressure by reducing the clock frequency, but they are limited by thermal noise and the 1/f noise floor, making it difficult to achieve an effective resolution of 16 bits or more with stable output under a sub-milliwatt budget. In recent years, research has focused on leveraging architectural innovation and process co-optimization to reduce energy consumption while maintaining high accuracy. For instance, Li Yujia et al. designed an integrated temperature sensor that uses a first-order Σ-Δ modulator, reducing 1/f noise through full differential chopping amplifiers, achieving 13 bits of effective resolution at 200 kHz with a clock frequency in 0.18 μm CMOS process, consuming only 0.18 mW of power, and with a resolution of 0.03°C, achieving high energy efficiency. [15] Such progress is attributed to the application of low-leakage transmission gates in switched-capacitor integrators and the optimized gating clock of digital decimation filters, effectively suppressing the dual growth of static and dynamic power consumption.

In extreme low-power scenarios such as IoT edge nodes, the energy efficiency disadvantage of Delta-Sigma ADCs is still evident. The average power consumption of its architecture is generally higher than 2 μW at resolutions above 12 bits, while SAR or TDC solutions typically control within 1 μW under the same precision. Therefore, its applications are mostly concentrated on industrial temperature measurement or battery management systems where precision requirements are strict and power supply is relatively relaxed. To balance accuracy and power consumption, a hybrid architecture trend has emerged in recent years: for example, combining ΔΣ modulators with TDC to achieve high-gain integration in the time domain, avoiding high-power amplifiers; or using configurable-order ΔΣ, operating in a reduced-order mode during standby to save energy.

4.2 Power Consumption Optimization Strategies for Digital Filters

4.2.1 Precision adaptive mechanism of cic and fir cascade structure

In the digital post-processing chain of CMOS temperature sensors, the cascaded structure of CIC (Cascaded Integrator-Comb) and FIR (Finite Impulse Response) filters is widely used to suppress out-of-band noise and improve the effective resolution. In recent years, to meet the strict energy efficiency requirements of the Internet of Things and wearable devices, researchers have proposed an accuracy adaptive mechanism, enabling the filters to dynamically adjust their working mode based on the current temperature change rate or the system power consumption budget. For example, when the environmental temperature is stable, the system

can reduce the order of the FIR filter or shut down some CIC cascaded units, thereby significantly reducing the computational load and switching activities. Zhao Yiqiang and Zhao Xinyu from Tianjin University, among others, proposed an accuracy adaptive digital sampling filter in their design work, which can select four different precision states based on the difference between the measured temperature and the threshold temperature. The test results show that when the filter switches from the highest precision state A to the lowest precision state D, the power consumption of the digital part of the sensor decreases from 71.55 μW to 63.44 μW, reducing by up to 11.3%. The implementation of the accuracy adaptive mechanism relies on the prior modeling of the statistical characteristics of the temperature signal. Industrial data shows that in most application scenarios (such as smart wristbands, battery management systems), the temperature change rate is usually lower than 0.1°C/s, which means that the high-frequency components are very weak and does not require continuous activation of high-order filtering. Therefore, after 2020, many studies proposed to use CIC as a rough anti-aliasing filter, and only activate the high-order FIR for fine compensation when a rapid temperature change is detected.

4.2.2 Filter reconstruction in single conversion mode and off-load shutdown mode

In the periodic wake-up type CMOS temperature sensor, the system is in a deep sleep state for most of the time, and only completes a single temperature conversion within a predetermined time window. This working mode imposes special requirements on the digital filter: it must ensure the noise suppression capability during a single sampling and completely turn off during non-working periods to avoid leakage power loss. To this end, researchers have proposed a filter reconfiguration mechanism, which dynamically configures the filter structure each time it wakes up and only enables necessary resources to complete the current conversion task. For example, after a single SAR ADC output, the system can select to enable a first-order CIC or short-tap FIR based on the preset noise tolerance, rather than maintaining a complete filter chain. Zhao Yiqiang and Zhao Xinyu from Tianjin University, among others, in their design of a low-power digital filter for CMOS temperature sensors, adopted a low-power working mode, dividing temperature monitoring into a single temperature conversion (STC) stage and an idle shutdown (IS) stage.

The key to filter reconfiguration lies in fast configuration and state retention techniques. Since the wake-up interval can be several seconds or even minutes, the internal registers of the filter need to save the key states (such as the accumulator value of the integrator) before shutdown and quickly restore them during the next startup. In recent years, configuration caches based on non-volatile storage units (such as eFlash or RRAM) have been introduced to avoid reloading coefficients each time the system restarts.

4.3 System-Level Low-Power Architecture Design

4.3.1 Periodic waking up and event-driven power management strategy

In the context of the rapid development of the Internet of Things and wearable devices, the CMOS temperature sensor, as a key sensing unit, its average power consumption directly affects the battery life of the terminal device. According to the global wearable device market report released by IDC in 2023, more than 76% of smart wristbands and health monitoring devices require that the sensor's standby current be lower than 100 nA to support a battery life of several months or even a year. To meet this stringent requirement, the periodic wake-up mechanism has become one of the core strategies in system-level low-power design. This mechanism uses an internal low-power real-time clock (RTC) or oscillator to wake up the sensor for a temperature sampling and conversion at a preset time interval, and then puts the entire system into deep sleep mode for the rest of the time. The key to this design lies in optimizing the balance between the wake-up period and the application accuracy requirements. An overly long period can further reduce power consumption, but it may miss temperature change events, while an overly short period can weaken the energy-saving effect. Therefore, in recent years, research has tended to introduce adaptive wake-up strategies, adjusting the sampling frequency dynamically based on the historical temperature change rate, to achieve maximum energy efficiency while ensuring data validity.

The event-driven power management strategy further breaks through the limitation of fixed cycles, directly linking power consumption control with external environmental changes.

This method usually combines threshold detection circuits or lightweight comparators to trigger system activation when the temperature deviates from the set range, and remains in a deactivated state otherwise. A study by the University of Electronic Science and Technology of China in 2022 showed that a CMOS temperature sensor with an accuracy-adaptive digital extraction filter architecture can selectively deactivate the arithmetic units in the filter based on the difference between the measured temperature and the set threshold temperature. When the measured temperature is outside the threshold temperature range, the digital part of the sensor's power consumption can be reduced by up to 11.3% to achieve a similar event-driven low-power effect. [6]

4.3.2 Analysis of the impact of quick startup circuit on average power consumption

In the periodic wake-up or event-driven working mode, the CMOS temperature sensor needs to go through a startup process from deactivation to stable operation each time it is activated. If the startup time is too long, it not only prolongs the effective working period but also significantly increases the average power consumption due to the high transient current during the transition stage. In the low-frequency wake-up scenario of 0.1–10 Hz, the startup energy consumption is the main body of the energy consumption for a single sample, as shown by the measured data from Texas Instruments (TI) and multiple academic studies. This proportion generally exceeds 30%. Therefore, the design of a fast startup circuit becomes a key link in system-level low-power optimization. In recent years, researchers have significantly shortened the stabilization time through technologies such as pre-biasing hold, capacitor energy storage, and loop acceleration. Tang Zhong et al. proposed a capacitor-reused direct voltage-to-duty cycle converter in 2018. This solution completes the short-term capacitor reset before each phase starts within a short period, using a single capacitor to complete the voltage-to-duty cycle conversion. Compared with existing solutions, this design not only reduces the capacitor area by 50% but also has no capacitor matching error in principle, improving the accuracy.

The improvement effect of the fast startup technology on average power consumption is particularly significant in the low-frequency wake-up scenario. This is mainly due to the effective suppression of the peak current during the startup stage and the shortening of the stabilization time, thereby reducing the duration of the high-power transition state. However, the fast startup circuit itself also requires extremely low static power consumption; otherwise, it will offset its energy-saving benefits. Therefore, modern designs generally use sub-threshold MOS switches to control the charging and discharging path of the energy storage element to ensure that the leakage current during the turn-off period is at the nanohertz level. In addition, the influence of process angle and temperature variation on the startup reliability is also not negligible. Some advanced solutions introduce a digital calibration mechanism, storing bias parameters after the first startup and directly calling them for subsequent wake-ups, further enhancing robustness. With the increasing demand for immediate response from IoT nodes, fast startup has evolved from an auxiliary function to the core indicator of system energy efficiency. Its deep integration with low-power architectures will continue to drive CMOS temperature sensors to move towards nanowatt-level average power consumption.

4.3.3 Communication energy consumption optimization for single-bus interface protocol

In resource-constrained IoT terminals, the energy consumption of communication interfaces often accounts for more than 20% of the total system power consumption. Especially for nodes that only need intermittent transmission of temperature data, simplifying the interface structure becomes an important way to reduce the overall power consumption. The single-bus protocol, due to its requirement of only one data line to serve as both the power supply and communication channel, significantly reduces the number of pins and peripheral components, thus becoming the mainstream interface choice for CMOS temperature sensors. Among the low-power temperature sensors shipped globally, the proportion using the single-bus interface is gradually increasing, highlighting its comprehensive advantages in energy efficiency and cost. This protocol extracts energy from the data line through the parasitic power mode, eliminating the need for dedicated power supply pins, enabling the sensor to operate without a local battery.

5. Conclusion

5.1 Summary of Main Research Findings

This study systematically reviewed the key technical paths for low-power optimization of CMOS temperature sensors, and demonstrated the multi-dimensional collaborative design logic from the device level to the system level. In the temperature sensing front-end, the sub-threshold MOSFET, with its exponential current-temperature characteristic, can achieve high sensitivity temperature measurement at nanohenry-level static bias, and combined with dynamic bias technology, further compresses the average power consumption to less than one-tenth of the traditional scheme. The research shows that in 65 nm and below process nodes, this method can control the linear error within ±0.5°C in the range of 25–85°C, and the static current is as low as 50 nA. The signal conditioning stage eliminates the traditional high-power operational amplifier and adopts a design integrating switch capacitor structure and chopping stabilization technology, effectively suppressing 1/f noise while avoiding introducing additional static power consumption. Especially in the past five years of research, this solution has achieved an input reference noise lower than 5 μVrms in 0.18 μm CMOS process, significantly outperforming similar circuits without using chopping technology.

At the analog-to-digital conversion and system architecture level, it was found that the time-domain conversion strategy (such as voltage-time conversion combined with TDC) is more suitable for ultra-low power consumption scenarios than the traditional SAR ADC. Fan Xudong from Hangzhou University of Electronic Technology designed a CMOS temperature sensor based on an RC oscillator in 2017, adopting a simplified architecture of oscillator plus counter. In TSMC 0.18 μm CMOS process, the temperature measurement accuracy in the range of -10°C to 80°C is ±3°C, the working voltage is only 1.2V, and the enable control signal is used to achieve software shutdown, effectively reducing idle state power consumption. Overall, the multi-module collaborative optimization not only breaks through the power consumption bottleneck of a single circuit improvement, but also promotes the application of CMOS temperature sensors in emerging fields such as IoT nodes, smart wristbands, and battery management systems of electric vehicles, providing solid technical support for high-integration and long-life sensing systems.

5.2 Current Research Limitations

Although current research has made significant progress in the low-power optimization of CMOS temperature sensors, there are still several limitations. Firstly, most literature focuses on reducing the power consumption of a single module, such as optimizing the temperature sensing front-end or ADC, lacking systematic verification of the collaborative design of the entire chain, which limits the overall energy efficiency improvement. Secondly, although sub-threshold MOSFETs can achieve nanohenry-level static current, their linearity and stability are difficult to guarantee under process variations, temperature drift, and power supply fluctuations. Especially in advanced process nodes below 65 nm, the parameter dispersion of the devices intensifies, affecting the consistency of mass production. Secondly, dynamic bias and periodic wake-up strategies effectively reduce the average power consumption, but frequent switching can introduce startup delays and transient errors, making it difficult to meet the requirements of high real-time applications. Additionally, existing noise suppression schemes mostly rely on chopping stabilization and switch capacitor structures, although they avoid using high-power amplifiers, they may introduce additional non-ideal effects due to clock feedback and charge injection, especially in ultra-low power conditions where the signal-to-noise ratio deteriorates significantly. Finally, current research is mostly based on simulation or small-scale prototyping verification, lacking long-term reliability data in real-world IoT or wearable device environments, and most power consumption indicators are not tested under unified conditions (such as sampling rate, resolution, process node), making it difficult to compare different solutions horizontally. There is still a gap between industry and theory.

5.3 Prospects for Future Research Directions

With the rapid development of the Internet of Things, wearable devices, and implantable medical electronics, the power consumption requirements for CMOS temperature sensors have approached the picowatt level. Although existing research has made significant progress in sub-threshold front-end, time-domain ADC, and system-level power management, further

exploration is still needed in multi-dimensional collaborative optimization. Firstly, at the device level, new temperature sensing structures should be developed in combination with advanced process nodes, using body effect or gate-induced voltage to enhance sensitivity while suppressing nonlinear errors caused by process angle deviations. Secondly, in the circuit architecture, adaptive resolution ADC technology needs to be developed urgently, enabling it to dynamically adjust the quantization bit according to environmental temperature changes, minimizing energy consumption while maintaining accuracy. Moreover, although the current combination of chopping stabilization and switch capacitor filters effectively suppresses 1/f noise, it is still limited by the lower limit of thermal noise in ultra-low frequency applications. Future research can explore full-digital noise suppression schemes based on time interleaving or correlated double sampling to completely 摆脱 the reliance on analog amplifiers. At the system level， the existing periodic wake-up mechanisms mostly rely on external clocks， introducing additional power consumption. Future research should study event-driven asynchronous sensing architectures，triggering conversions only when temperature changes occur， achieving true "zero standby" power consumption. Future research should focus on cross-level collaborative design ， connecting the optimization loop from device physical characteristics to system behavior models， and promoting the large-scale deployment of CMOS temperature sensors in energy-constrained scenarios.

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