Design and Implementation of Radar IF Signal Processing Board Based on PPC+DSP+FPGA Architecture

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Abstract: Next-generation radar systems impose stringent requirements on signal processing units, including high real-time performance, high sampling accuracy, high-speed data exchange, and strong environmental adaptability. To address these challenges, this paper designs and implements an integrated radar processing board based on a heterogeneous collaborative processing architecture consisting of PPC, DSP, and FPGA. The board integrates multiple functions such as parallel multi-channel IF signal acquisition, high-precision waveform generation, high-speed optical fiber communication, remote program loading, and system health management. Systematic optimizations are carried out at three levels: hardware link, logic timing, and software architecture, the module strictly complies with military equipment design specifications and has passed environmental adaptability verifications including electromagnetic compatibility, high/low temperature operation (–55 °C to +70 °C), vibration, and shock tests. It can be stably adapted to various complex combat scenarios such as airborne, shipborne, vehicle-mounted, ground fixed stations, and electronic countermeasures. Measured results show that the ADC achieves an effective number of bits (ENOB) of 12.3 bits, the DAC phase noise is better than –105 dBc/Hz@1 kHz, and the data bandwidth between the FPGA and DSP via the SRIO interface reaches 20 Gbps. All specifications are better than the design expectations, fully meeting the multi-task processing requirements of radar target detection, tracking, imaging, and electronic countermeasures. The work presented in this paper provides a high-performance and highly reliable hardware processing platform for advanced radar systems, offering significant engineering application value and promising prospects for further adoption.

Keywords: Radar Integrated Processing Board; Heterogeneous Processing Architecture; PPC+DSP+FPGA; High-Speed Signal Acquisition; Optical Fiber Communication; Military Radar; Multi-Scenario Adaptability

1. Introduction

In modern electronic warfare and information-based combat systems, radar equipment is rapidly evolving toward multi-function integration, miniaturization, low power consumption, and high reliability. As a core component of electronic information systems, the radar signal processing unit must simultaneously perform multiple complex parallel tasks, including digitized acquisition of IF analog signals, broadband waveform generation, real-time processing of massive data, high-speed interconnection and data exchange among multiple devices, as well as remote control and management. As a result, the system imposes extremely high requirements on processing capability, computation speed, sampling accuracy, transmission bandwidth, and environmental adaptability.

Traditional radar signal processing boards generally adopt a single-processor architecture or a separate “acquisition-processing” design. In practical applications, such approaches suffer from insufficient computing power, redundant interfaces, complex links, high power consumption, high failure rates, and poor environmental adaptability. For example, a solution relying solely on a DSP or an FPGA struggles to balance complex algorithmic computation with system control and management. Meanwhile, a separate acquisition-processing design leads to large board-level interconnection latency and weak anti-interference capability, making it difficult to meet the requirements for continuous, stable, and efficient data processing in complex battlefield environments.

To address the above issues, this paper

constructs a heterogeneous collaborative processing architecture based on the P1010 PPC, TMS320C6678 DSP, and Kintex-7 FPGA, and designs an integrated radar processing board [1]. This solution streamlines hardware links, enhances computational efficiency, and improves system reliability. It is suitable for multi-platform, multi-scenario radar applications and fully meets the core task requirements of target detection, trajectory tracking, synthetic aperture imaging, and anti-jamming signal processing. Furthermore, by reasonably partitioning control, computation, and logic resources, the design achieves an engineering-feasible balance among performance, power consumption, and size, providing a practical and effective hardware solution for next-generation military and high-end civilian radar systems.

2. Typical Application Scenarios

This radar processing board adopts a modular, ruggedized design and fully covers military and high-end civilian radar application scenarios. It mainly includes: airborne early warning and fire control radar – suitable for high-altitude low temperature, strong vibration, and limited power supply, supporting rapid target detection, multi-target tracking, and fire control command exchange; shipborne surface/air search radar – meeting long-term stable operation under high salt spray, high humidity, and strong electromagnetic interference, enabling sea surface search, low-altitude interception, and weapon guidance; vehicle-mounted mobile radar – adapting to road bumps, wide temperature ranges, and rapid mobility, supporting remote unattended management in field environments; ground fixed/border surveillance radar – withstanding extreme temperatures and uninterrupted operation, performing long-range warning and intrusion detection; electronic reconnaissance and anti-jamming radar – leveraging high-speed acquisition and real-time processing capabilities to achieve signal capture, jamming waveform generation, and spectrum analysis.

2.1 Airborne Early Warning and Fire Control Radar Scenarios

It is mainly suitable for platforms such as fighter aircraft, early warning aircraft, and helicopter airborne radars, and is capable of operating in harsh environments including high-altitude low temperatures, severe vibration, and limited onboard power supply. It can perform rapid detection of aerial targets, multi-target tracking, identification friend or foe (IFF), and generation of fire control command signals. It supports high-speed data exchange between the radar and the airborne fire control system as well as the communication system, offering advantages such as small size, low power consumption, and strong vibration resistance.

2.2 Shipborne Surface-Search / Air-Search Radar Scenarios

Applied to destroyers, frigates, and shipborne early warning radar systems, it adapts to maritime environments with high salt spray, high humidity, and strong electromagnetic interference. It features good anti-corrosion design and electromagnetic compatibility (EMC), and can perform sea surface target search, interception of low-altitude penetrating targets, and guidance signal processing for shipborne weapon systems, supporting long-term continuous and stable operation.

2.3 Vehicle-Mounted Mobile Radar Scenarios

It is mainly suitable for vehicle platforms such as field communication vehicles, air defense radar vehicles, and mobile reconnaissance vehicles. It can meet the mobility requirements including road bumpiness, wide-temperature operation, and rapid deployment/retraction. It also supports remote program loading and status monitoring for unattended field operation, and can perform signal processing tasks such as ground target reconnaissance, low-altitude drone defense, and battlefield situational awareness.

2.4 Ground Fixed / Border Surveillance Radar Scenarios

It is mainly used in fixed-station radar systems such as border line monitoring, key point air defense, and environmental meteorological detection. It can adapt to extreme high/low temperatures and long-term continuous operation requirements. It also enables long-range target detection, border intrusion alarming, and meteorological data acquisition and processing, while supporting remote operation/maintenance and fault self-diagnosis functions.

2.5 Electronic Reconnaissance and Anti-Jamming Radar Scenarios

It is mainly suitable for electronic countermeasure (ECM), spectrum monitoring, and radar anti-jamming systems. Relying on its high-speed acquisition and real-time processing capabilities, it can quickly capture enemy radar electronic signals, and perform jamming waveform generation, spectrum analysis, and interference suppression, thereby enhancing the survivability of radar systems in complex electromagnetic environments.

3. Overall Design and Functional Specifications

3.1 Overall Architecture

The processing board adopts a three-layer integrated architecture consisting of analog front-end acquisition, digital core processing, and external interface communication. The signal processing chain is as follows: IF echo → AD digitization → FPGA performs DDC (Digital Down Conversion), pulse compression, and data framing → DSP performs MTI (Moving Target Indication), MTD (Moving Target Detection), CFAR (Constant False Alarm Rate), and tracking → output target tracks. The core processors have clear task divisions and operate efficiently:

AD Converter (AD9467): Acquires the signal that has been filtered and mixed down to IF by the analog front end, converts it to a digital IF signal, and sends it to the FPGA [2].

FPGA (Kintex-7 325T): Logic control core. Implements ADC/DAC timing control, beam steering, data buffering, pulse compression, high-speed optical fiber transmission, and SRIO/PCIe interface data transfer [3].

DSP Processor (TMS320C6678): Algorithm computing core. Handles high-intensity operations such as radar signal filtering, MTI (Moving Target Indication), MTD (Moving Target Detection), CFAR (Constant False Alarm Rate), target condensation, target tracking, and imaging algorithms [4].

PPC Processor (P1010): System management and control core. Responsible for network communication, remote program loading, equipment status monitoring and reporting, fault self-diagnosis, peripheral scheduling, and sending track number, range, velocity, azimuth, and amplitude to the host computer via Ethernet [5].

The overall architecture block diagram is shown in Figure 1.

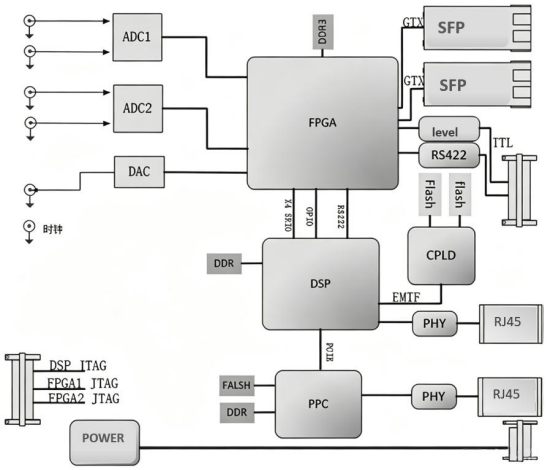

Figure 1. Block Diagram of the Overall System Architecture

3.2 Core Technical Specifications

Signal acquisition: 4-channel parallel acquisition of IF signals at 140±20 MHz, sampling rate 200 MSPS, quantization 14 bits.

Signal generation: 1-channel high-speed DA waveform output, maximum sampling rate 2.4 Gsps, output frequency 140±20 MHz.

Acquisition accuracy: ADC effective number of bits (ENOB) ≥ 11 bits (12 bits measured).

Output quality: DAC phase noise < –95 dBc/Hz @ 1 kHz (–105 dBc/Hz measured).

High-speed interconnection: FPGA-DSP SRIO bandwidth 20 Gbps, optical fiber transmission rate 6.25 Gbps.

Remote control: Supports remote program loading via Gigabit Ethernet.

Environmental adaptability: Operating temperature –55 °C to +70 °C, complies with GJB150/GJB151 military standards.

4. Key Hardware Design

4.1 Analog Front-End Signal Chain

IF input → impedance matching → anti-aliasing filter → ADC → FPGA → DSP → PPC → host computer.

Clock: high-precision crystal oscillator → clock driver → ADC/DAC synchronous clock.

4.2 Power Supply and Clock Architecture

External power → input filter → multi-channel DC/DC split-domain power supply.

Analog power → ADC / DAC.

Digital power → FPGA / DSP / PPC / peripherals / drivers.

High-precision crystal oscillator → clock distribution network.

ADC sampling clock.
DAC output clock.
FPGA/DSP synchronous clock.

4.3 Key Hardware Design Points

ADC/DAC front end: Uses AD9467 + AD9739 chips. Optimizes impedance matching and filtering, separates analog and digital domains, reduces crosstalk [6].
High-speed interface: FPGA and DSP communicate via SRIO at 20 Gbps; PPC uses PCIe for system scheduling [7].
Power and clock: Split-domain power supply, overcurrent protection, low phase-noise clock, ensures system-wide timing synchronization and stability.
EMC and mechanics: Complies with GJB151A-97, shielding grounding, filter isolation, ruggedized structure meets vibration and shock requirements [8].
PCB layout: Channel isolation, equal-length and symmetric ADC routing, impedance control, ensures signal integrity.

5. Logic and Software System Design

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5.1 FPGA Functional Modules

CPLD control module: Reset, loading, monitoring (9 voltages + 4 temperatures).
Acquisition module: ADC timing, data buffering, digital filtering.
Transmission module: DAC waveform control, gain, timing output.
High-speed interfaces: SRIO, Aurora, PCIe.
Beam steering interface: LVTTL driven via level shifters for control.

5.2 Software Hierarchy

Application layer: Health management, remote loading, command parsing, fault reporting.
Driver layer: Ethernet, PCIe, UART, Flash, DDR.
File system: dosFs + TrueFFS.
Operating system: VxWorks 7.0 [9].
Hardware layer: PPC, bus, memory, interfaces.

6. Environmental Adaptability and Reliability Design

6.1 Environmental Qualification Tests

High/low temperature operation: –55 °C to +70 °C.
Humidity, salt spray, fungus.
Vibration (sinusoidal + random).
Shock and drop.

6.2 Reliability Assurance Measures

Component selection: Military-grade / industrial-grade components with strict secondary screening.
Derating design: Voltage, current, and power derating for critical devices.
Thermal design: Optimized layout and heat dissipation paths to ensure long-term stable operation [10].
Quality control: Full-process inspection + burn-in screening, compliant with GJB9001B quality management system.

7. Test Results and Analysis

To verify whether the performance indicators of the radar IF signal processing board meet design requirements, comprehensive performance testing has been conducted on the system. The test results are shown in Table 1:

Table 1. System Performance Test Results

Test Item	Design Index	Measured Result	Test Conclusion
ADC ENOB	≥11bits	12bits	Qualified
DAC Phase Noise @1kHz	＜-95dBc/Hz	-105dBc/Hz	Qualified
FPGA-DSP Data Bandwidth	≥6.4Gbps	20Gbps	Qualified
Optical Fiber Transmission Rate	6.4Gbps	6.4Gbps	Qualified
High/LowTemperature Operation	-55℃~+70℃	Normal function	Qualified
Electromagnetic Compatibility	Complies with GJB151A-97	Passed	Qualified

As shown in Table 1, all measured specifications of the processing board are better than the design requirements. The ADC effective number of bits reaches 12 bits, which is more than 9% higher than the design target, ensuring the acquisition accuracy of weak signals. The DAC phase noise is better than –105 dBc/Hz @ 1 kHz, demonstrating excellent waveform output quality. The FPGA-DSP achieves high-speed data exchange at 20 Gbps via the SRIO interface, with a transmission bandwidth far exceeding the design threshold, meeting the

real-time processing requirements of massive radar data. Both high/low temperature and electromagnetic compatibility tests have been passed, confirming that the system has good environmental adaptability and reliability.

8. Conclusion

The radar IF signal processing board based on the PPC+DSP+FPGA architecture designed in this paper realizes integrated functions such as signal acquisition, waveform generation, high-speed processing, and remote management, offering high precision, high bandwidth, high reliability, and multi-scenario adaptability. The module fully meets the requirements of radar platforms including airborne, shipborne, vehicle-mounted, and ground fixed stations, and can support multi-task processing such as target detection, tracking, imaging, and electronic countermeasures, aligning with the development direction of next-generation military radar equipment. Future work will focus on further hardware-based algorithm integration, power consumption reduction, and size miniaturization, so that the radar signal processing board can be widely used in lighter, more highly integrated radar systems.

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