Optimization of Signal Source and Clock Source Combination for ADC Chip Test Based on V93000 Platform

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Abstract: In the development and verification of high-speed and high-precision Analog-to-Digital Converters (ADCs), the configuration of the test platform is critical for obtaining accurate and repeatable dynamic performance data. During the testing of a high-performance ADC, significant performance fluctuations were observed under different combinations of clock sources and signal sources, which affected the accuracy of performance evaluation and the stability of mass production testing. To address this issue, this paper optimizes the mixed-signal test platform through clock source selection and signal source matching. Based on the V93000 SmarTest 8 platform, this study investigates a high-speed 4- channel ADC with a resolution of 16 bits and a sampling rate of 125 Msps. Two clock schemes, namely Oscillator (OSC) and PS1600, as well as two signal sources, namely WaveScale MX (WSMX) and Signal Generator SMA100B, are comparatively studied. Key performance indicators, including Signal-to-Noise Ratio (SNR), Signal-to-Noise Ratio relative to Full Scale (SNR-dBFS), and Total Harmonic Distortion (THD), are evaluated under input frequencies of 10 MHz and 300 MHz. The experimental results demonstrate that OSC exhibits better phase noise and jitter performance than PS1600, while SMA100B provides higher spectral purity than WSMX. The optimal combination of OSC and SMA100B effectively reduces spectrum leakage and jitter interference, thereby achieving more stable ADC dynamic performance testing. This paper proposes an optimized test platform configuration scheme, which provides a reliable reference for ADC verification, load board design, and mass production testing.

Keywords: High-speed ADC; SMA100B; WSMX; PS1600; V93000; SmarTest 8.

1. Introduction

With the rapid development of 5G communications, high-speed data acquisition, radar systems and automotive electronics, the demand for high-speed analog-to-digital converters (ADCs) has been growing steadily. Dynamic performance metrics of ADC, including signal-to-noise ratio (SNR), Signal-to-Noise Ratio Relative to Full Scale (SNR-dBFS), total harmonic distortion (THD) serve as the critical criteria for chip design verification, performance grading and mass production testing. However, in practical measurement, these indicators are determined not only by the design and process of the chip itself, but also significantly affected by the test platform, such as clock quality and signal source purity. In many cases, the test platform itself becomes the bottleneck that restricts accurate characterization of chip performance.

In a mixed-signal test system, the clock source provides the timing reference for sampling. Clock jitter and phase noise directly introduce timing errors during sampling, resulting in degraded SNR and elevated noise floor. The signal source supplies the analog excitation to the ADC. Excessive harmonics and spurs in the excitation will overlap with the distortion generated by the ADC, making it impossible to distinguish the genuine performance of the device.

At present, most studies focus on the design and algorithm optimization of ADCs, whereas systematic and quantitative research on the configuration optimization of test platforms is relatively insufficient. In engineering practice, test engineers usually select instruments and set parameters based on experience without sufficient experimental comparison and theoretical support, which leads to large deviations between test results and actual performance, and even misjudgment of chip capabilities.

To address these issues, this paper takes a self-

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developed high-performance high-speed ADC as the device under test, and conducts comprehensive optimization on the test platform to resolve the performance anomalies observed during testing. The research mainly consists of three parts: first, comparing the performance of two clock sources, i.e., OSC and PS1600; second, analyzing the pros and cons of two signal sources, i.e., WSMX and SMA100B; third, performing combination tests of clock and signal sources to determine the optimal configuration. Through quantitative comparison of extensive test data and spectrum analysis, this paper proposes a practical and reliable configuration scheme for the test platform, which can provide guidance for high-precision ADC test and verification.

2. Test Platform Overview

Automatic Test Equipment (ATE) is a key tool in integrated circuit testing. It is used to simulate the operating conditions of a device under test (DUT) under various scenarios and compare its behavior with the expected operating states, thereby identifying potential chip defects [1].

An integrated circuit (IC) test platform primarily consists of test equipment and its supporting software system. The test equipment includes several hardware components, with its core functions being the generation of test stimulus signals and the acquisition and processing of signals from the device under test. The supporting software system is responsible for developing test programs and coordinating the operation of the test equipment by executing predefined test plans. This enables the evaluation of the chip's electrical characteristics and functional specifications, as well as the recording, processing, and storage of test data [2].

2.1 Advantest V93000 Overview

The V93000 is a test system developed by Advantest for use on a scalable platform. It integrates high-speed digital testing, precision analog testing, and radio-frequency (RF) measurement resources. Most of the testing functions are integrated into the test head, allowing the V93000 to deliver maximum speed while significantly reducing intrinsic hardware noise. Each type of test hardware card is highly integrated, and the management and configuration of different test resources within the test head are distributed. This enables the V93000 SoC test system to provide excellent flexibility [3]. The V93000 ATE is widely used in SoC chip testing and has become an important test system for wafer-level testing (CP test) and final test (FT test). Wafer-level testing mainly focuses on DFT and functional testing, while final test mainly performs functional and parametric measurements [4,5]. Some of these test items involve the test program methods of the V93000 tester, including general test programs such as functional testing, AC parameter testing, DC parameter testing, and dynamic power (Pdyn) testing[6].

2.2 SmarTest 8 PlatForm Overviw

SmarTest is the software package for the V93000 test system series and is based on the Linux operating system. Test program development is carried out through this software. It supports the development of digital, analog, mixed-signal, and RF test programs. The software controls the hardware to perform actions such as supplying current, applying voltage, and generating arbitrary waveform signals to the device under test (DUT), and it also handles data processing, fault analysis, and system diagnostics based on the acquired measurement data [7].

3. Clock Source Application and Performance Analysis

In a mixed-signal test system, the clock source represents one of the most critical modules. It determines the sampling timing accuracy of the ADC and directly affects the dynamic performance of the entire system. An ideal clock signal should feature ultra-low jitter, low phase noise, high stability, and excellent signal integrity. In this project, the ADC employs a 125 MHz differential clock with a peak-to-peak voltage of 1.6 V and a sinusoidal waveform. The clock signal is connected to the CLKin+ and CLKin− pins of the chip via relays on the load board, and can be switched between different clock sources (OSC and PS1600) for convenient comparison.

3.1 OSC Clock Analysis and Application

Crystal oscillator (OSC) is the most widely used clock source in integrated circuits. An active crystal oscillator is an electronic oscillation device based on the piezoelectric effect of a quartz crystal, with transistors, resistors, capacitors, and other components integrated

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internally to form a complete oscillation system [8]. Its significant advantages include eliminating the need for external oscillator matching, strong anti-interference capability, and a high signal-to-noise ratio. It is widely used in communication equipment, embedded systems, and other fields with stringent timing requirements. Moreover, by integrating filter capacitors and driver circuits, it significantly improves the signal-to-noise ratio, making it a core device for clock references in modern electronic equipment [9].

The OSC used in this test is a factory-calibrated fixed-frequency oscillator, which can directly generate a 125 MHz clock without an external input signal. It adopts a standard four-pin package including power supply, ground, clock output, and enable control. The internal circuit consists of a crystal chip, an oscillation circuit, an amplifier, and a shaping circuit, which can provide stable differential clock output.

The advantages of OSC are significant: first, it has a simple structure and does not require complex software configuration; second, it exhibits low phase noise and small jitter in the middle and low frequency bands; third, it operates stably and is less affected by the internal noise of the test equipment. Nevertheless, its disadvantages are also prominent: the output frequency is fixed and its flexibility is poor, meaning the frequency cannot be adjusted in real time according to test requirements. Therefore, changing the frequency necessitates replacing the crystal oscillator or mounting multiple oscillators on the load board, which consumes valuable layout space.

In low-frequency test scenarios close to actual application environments, OSC can well meet the test requirements and provide a stable and reliable clock signal for the ADC.

3.2 PS1600 Clock Analysis and Application

The PS1600 is a digital board inside the ATE test system, which can be used as both a measurement resource and a programmable clock source. The PS1600 digital channel card provides a total of 128 digital channels, supporting a higher number of pin tests and greater multi-site testing capability, thereby reducing infrastructure usage and overall cost [10]. On the SmarTest 8 test platform, the PS1600 can be employed as a clock source and configured with multiple parameters.

In this project, the PS1600 is configured to output a 125 MHz differential sinusoidal clock with a peak-to-peak voltage of 1.6 V, consistent with the output parameters of the OSC. The clock generated by the PS1600 can be strictly synchronized with the digital vectors and data acquisition units of the test system, which helps improve test repeatability and prevent spectrum leakage. Meanwhile, as an internal digital board of the ATE tester, the PS1600 features flexible programmability and can be dynamically adjusted to output different frequencies, peak-to-peak voltages, DC bias levels, and operate in single-ended or differential modes according to test requirements.

However, the PS1600 clock is derived from the internal frequency synthesis and clock distribution network of the ATE, which introduces relatively high phase noise and jitter, especially in the high-frequency band. In addition, internal power supply noise, inter-board crosstalk, and signal routing also degrade the final clock quality.

In summary, the PS1600 clock offers high flexibility and good system integration, making it suitable for conventional functional verification and mass-production testing with low performance requirements. Nevertheless, its clock quality may become a performance bottleneck in high-precision dynamic performance tests for high-speed ADCs.

4. Signal Source Application and Performance Analysis

The signal source provides the analog input excitation for the ADC, and its spectral purity, amplitude accuracy, frequency range and flatness directly determine the reliability of indicators such as THD and SNR. Two signal sources are adopted in this test platform: the onboard WSMX board and the external high-performance RF signal generator SMA100B. The WSMX and SMA100B are both used in the 10 MHz low-frequency test, while only the SMA100B can be used in the 300 MHz high-frequency test due to the bandwidth limitation of the WSMX board. Coherent sampling is employed in the test to avoid spectrum leakage, with a sampling point count of 16384 and a sampling frequency of 125 MHz.

4.1 WSMX Signal Source Analysis and Application

WSMX (WaveScale MX) is a high-speed signal generation board integrated into the ATE system.

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It features high frequency resolution, precise amplitude adjustment and multi-site parallel output capability, and can be programmed and controlled via SmarTest 8 software to realize automatic parameter switching.

The output signal of WSMX is transmitted to the analog input port of the ADC through 50 Ω impedance-matched high-frequency coaxial cables and filter networks. To reduce signal reflection and transmission loss, the entire signal path adopts continuous impedance design. In this experiment, the actual output frequency is set to 10.00213623046875 MHz according to the coherent sampling formula, which ensures that the input signal contains an integer number of cycles within the sampling window and effectively suppresses spectrum leakage.

Although the WSMX board is easy to use, highly integrated and applicable to multi-site parallel testing, it has obvious performance limitations in high-performance ADC testing. Its output signal contains prominent harmonics and spurious components with a relatively high noise floor. Meanwhile, it is restricted by narrow bandwidth and cannot generate high-frequency signals up to 300 MHz.

4.2 SMA100B Signal Source Analysis and Application

The SMA100B is a high-performance RF signal generator developed by Rohde & Schwarz. It features ultra-low phase noise, high frequency stability, excellent spectral purity and a wide output frequency range, and is widely adopted in high-precision measurement fields including chip testing, radar verification and communication testing.

In this paper, the SMA100B is adopted as the external signal source to generate high-purity sinusoidal signals at 10 MHz and 300 MHz. It communicates with the host computer of the ATE system via GPIB bus, and remote control over frequency, amplitude, on-off state and other parameters can be realized by sending SCPI commands through test programs.

To satisfy the coherent sampling conditions, its output frequencies are accurately set to 10.00213623046875 MHz and 299.99542236328125 MHz respectively. The entire signal transmission path adopts 50 Ω impedance matching design, and the signal is distributed to two test stations through a power divider.

Compared with the WSMX board, the SMA100B possesses remarkable superiorities. Firstly, it has ultra-low phase noise and low noise floor, which avoids introducing extra noise interference to the whole test system. Secondly, its extremely low harmonic distortion can truly reflect the inherent distortion characteristics of the ADC chip. Thirdly, it covers a broad frequency range and supports high-frequency testing at 300 MHz and above. Nevertheless, it also has certain drawbacks. Additional dedicated interfaces need to be designed on the load board for matching this signal source. Besides, as an external test instrument, it requires field staff to master relevant installation and commissioning skills in practical mass production applications.

5. Combination Optimization of Clock and Signal Source

The dynamic performance of ADC is the result of the joint action of clock source and signal source. Clock jitter affects sampling timing accuracy, and signal source purity affects input distortion. In order to find the optimal configuration, this paper combines two clock sources and two signal sources for full factorial comparison test. Before the test, the ADC has completed channel interleaving calibration and burned the calibration parameters into eFuse to eliminate the impact of interleaving mismatch.

5.1 Performance Comparison at 10 MHz Input

At the input signal frequency of 10 MHz, the test results of ADC channel 1 under different combinations are shown in Table 1.

It can be seen from the table that under the 10 MHz signal, the combination of OSC clock and SMA100B signal source achieves the best performance, with the highest SNR and the lowest THD. The SNR of PS1600 plus WSMX combination is the lowest and the distortion is the most serious.

From the perspective of mechanism, in the low-frequency band, the clock jitter has relatively little impact on SNR, and the signal source purity plays a leading role. SMA100B provides higher signal purity than WSMX, so the test results are better. At the same time, OSC has lower phase noise than PS1600, which further improves the test performance.

The spectrum analysis (Figure 1) shows that when OSC and SMA100B are used, the noise floor of the whole spectrum is low, the energy of the main frequency signal is concentrated, the

harmonic component is small, and the waveform is clean.

Table 1. ADC Channel 1 Performance under 10 MHz Input with Different Clock and Signal Source Combinations

Configuration	SNR	SNR_DBFS	THD
OSC_125M_SMA100B	74.82	75.94	-78.29
PS1600_125M_SMA100B	64.74	65.86	-77.27
OSC_125M_WSMX	72.07	73.19	-76.91
PS1600_125M_WSMX	59.01	59.09	-74.05

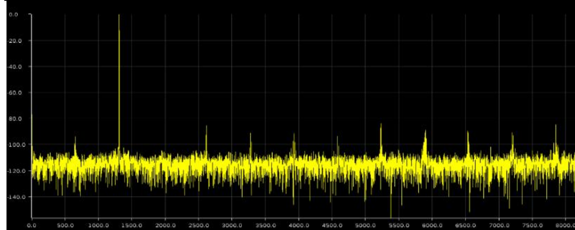

Figure 1. OSC Serving as Clock Source and SMA100B Serving as Signal Source under 10 MHz Input Signal Condition

In comparison, when the PS1600 is used as the clock source, the frequency-domain spectrum (Figure 2) shows a noticeable increase in the noise floor, and the noise components in certain high-frequency regions become more pronounced. This indicates that the phase noise and jitter of the clock source may have a more significant impact on the sampling stability of the ADC. Therefore, in low-frequency dynamic performance testing scenarios, a crystal oscillator clock source can better meet the requirements for high-precision sampling and provide a more reliable data basis for subsequent dynamic parameter analysis.

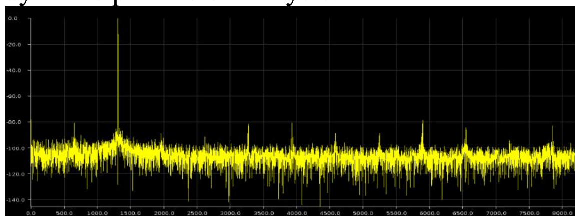

Figure 2. PS1600 Serving as Clock Source and SMA100B Serving as Signal Source under 10 MHz Input Signal Condition

When WSMX is used as the signal source (Figure 3), it can be observed that the signal-to-noise ratio (SNR) of the ADC output is significantly lower than that obtained when SMA100B is used as the signal source. This indicates that, although the WSMX board is capable of serving as a signal source for basic dynamic performance testing, it exhibits insufficient performance when applied to high-resolution, high-speed ADCs and is unable to reveal the intrinsic performance limits of the device. This result provides important guidance for load board design and resource allocation in high-performance ADC testing.

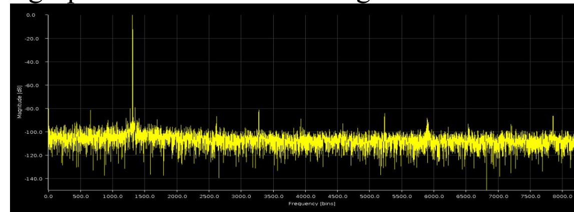

Figure 3. OSC Serving as Clock Source and WSMX Serving as Signal Source under 10 MHz Input Signal Condition

5.2 Performance Comparison at 300 MHz Input

Since WSMX cannot output 300 MHz signals, only SMA100B is used as the signal source at high frequencies to compare the performance of OSC and PS1600 clocks. The results are shown in Table 2.

The data shows that at 300 MHz, the performance difference between OSC and PS1600 is greatly enlarged. The SNR of OSC clock is nearly 25 dB higher than that of PS1600, and THD is significantly better. This is because with the increase of input signal frequency, the influence of clock jitter on SNR becomes more significant. The jitter performance of PS1600 is poor, resulting in serious sampling timing error, increased noise floor, obvious spectrum leakage and sharply deteriorated distortion indicators.

The spectrum diagram (Figure 4) shows that when PS1600 is used as the clock, the second harmonic is significantly increased, the noise around the main frequency is large, and the waveform quality is seriously degraded. When OSC is used, the spectrum (Figure 5) is clean, the harmonic is low, and the dynamic performance is good.

Table 2. ADC Channel 1 Performance under 300 MHz Input with Different Clock and Signal Source Combinations

Configuration	SNR	SNR_DBFS	THD
OSC_125M_SMA100B	63.4	66.96	-69.414
PS1600_125M_SMA100B	38.59	42.04	-38.12

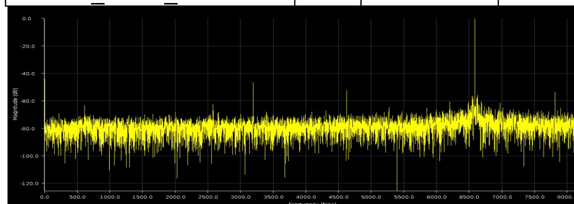

Figure 4. Output Spectrum of Channel 1 with PS1600 Serving as Clock and SMA100B as Signal Source under 300MHz Signal Condition

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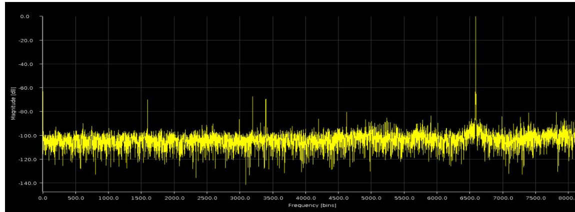

Figure 5. Output Spectrum of Channel 1 with OSC Serving as Clock and SMA100B as Signal Source under 300 MHz Signal Condition

6. Recommended Clock and Signal Source Combination Strategy for High-Speed ADC Dynamic Performance Testing

Based on the test results obtained under both low-frequency and high-frequency scenarios, the optimal clock-source and signal-source combination scheme for high-speed ADC dynamic performance testing can be summarized as follows:

(a)For low-frequency test scenarios (e.g., 10 MHz), the combination of the OSC clock and SMA100B signal source should be prioritized. This configuration achieves the highest SNR and the best THD performance, enabling accurate characterization of the ADC dynamic performance. If the testing requirements are relatively relaxed and greater emphasis is placed on testing efficiency and cost control, the combination of the OSC clock and WSMX signal source can be adopted to satisfy conventional functional verification requirements.

(b)For high-frequency test scenarios (e.g., 300 MHz), the combination of the OSC clock and SMA100B signal source must be adopted. Due to jitter and phase-noise limitations, the PS1600 clock cannot satisfy the requirements of high-precision testing. Meanwhile, the WSMX signal source cannot output high-frequency signals because of its bandwidth limitations. Therefore, neither of them is suitable for high-frequency test scenarios.

(c)For mass-production testing scenarios, if the objective is conventional functional verification with low testing cost, the combination of the PS1600 clock and WSMX signal source may be selected for low-frequency testing. However, when testing accuracy must be guaranteed and high-performance chips need to be accurately screened, the combination of the OSC clock and SMA100B signal source should be adopted to ensure that the test results can faithfully reflect the intrinsic performance of the ADC.

7. Conclusion

This study focused on the configuration optimization of clock sources and signal sources in high-speed ADC test platforms. Combination tests were carried out using two clock sources, OSC and PS1600, together with two signal sources, WSMX and SMA100B. Through dynamic performance testing and spectrum analysis under 10 MHz and 300 MHz scenarios, the following conclusions were obtained:

(a)The combination of clock source and signal source has a decisive influence on the dynamic performance test results of high-speed ADCs. In both low-frequency and high-frequency scenarios, the OSC clock demonstrated better testing performance than the PS1600 clock, while the SMA100B signal source consistently outperformed the WSMX signal source.

(b)In low-frequency scenarios, the spectral purity of the signal source is the dominant factor affecting the test results, whereas the influence of clock jitter is relatively limited. In high-frequency scenarios, the impact of clock jitter becomes significantly more pronounced and turns into the key factor limiting test accuracy. The jitter and phase noise characteristics of the PS1600 clock make it unable to satisfy the requirements of high-precision testing under high-frequency conditions.

(c)The combination of the OSC clock and SMA100B signal source was identified as the optimal testing solution. In the 10 MHz scenario, the SNR reached 74.82 dB and the THD reached −78.29 dB, while in the 300 MHz scenario, the SNR reached 63.4 dB and the THD reached −69.414 dB. This combination effectively suppresses noise and spectral leakage, thereby accurately reflecting the intrinsic dynamic performance of the ADC.

Therefore, when linear dynamic switching of clock frequency is not required and sufficient space is available on the load board, crystal oscillators should be preferentially selected as the clock source for ADC testing. For chips with higher resolution and higher input signal frequencies, the SMA100B should be prioritized as the external signal source. The combination optimization scheme proposed in this study addresses the existing issues of experience-based instrument selection and insufficient testing accuracy in high-speed ADC testing, providing a reliable engineering reference for the verification and mass-production testing of high-

performance ADCs.

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