Transforming Competition Challenges into Pedagogical Assets: A PBL Framework for Vocational Undergraduate Electronics Education

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Abstract: The National Undergraduate Electronics Design Contest (NUEDC) is the most influential electronics competition in China, yet its rich engineering challenges are rarely systematically transformed into curriculum-aligned pedagogical resources. This paper proposes the Project-Contest-Lifting (PCL) pipeline, a five-stage framework that converts competition tasks into project-based learning (PBL) modules anchored in vocational undergraduate curricula. The PCL pipeline is governed by four design principles: Curriculum-Contract Mapping (CCM) ensures one-to-one correspondence between course knowledge units and learning modules; Difficulty-Monotone Module Ordering (DMMO) sequences modules by a Bloom-anchored difficulty coefficient α with the constraint α1 ≤ 0.3; Closed-Loop Metric Anchoring (CLMA) ties each assessment gate to verifiable competition specifications; and Auditory Feedback Loop (AFL) substitutes expensive spectrum analyzers with perceptual verification for resource-constrained programs. Three case studies spanning distinct technical domains-laser tracking (machine vision), sound-discriminating music systems (digital signal processing), and contactless control panels (multi-sensor fusion)-demonstrate the framework's transferability. Pre/post assessment data (N = 32 per cohort) show consistent large-effect gains (Cohen's d = 1.70–2.46, p < .001) across all competency dimensions. The framework offers a replicable pathway for vocational institutions to leverage competition heritage without reproducing competition-specific training.

Keywords: Project-based Learning; Engineering Education; Curriculum Design; Vocational Education; Bloom's Taxonomy; Competition-Derived Pedagogy; DSP Education; Embedded Systems

1. Introduction

1.1 The Competition–Curriculum Gap

The National Undergraduate Electronics Design Contest (NUEDC) draws over 40,000 participants per edition across tracks ranging from power electronics to machine vision [1]. Each problem statement is drafted by senior engineers together with university faculty, and specifies performance targets in engineering units - centimeters of tracking error, hertz of frequency tolerance - that students must meet. The 72-hour sprint requires a functional hardware prototype, which rules out simulation-only approaches. This combination of concrete metrics and time-bounded hardware delivery is why NUEDC tasks are chosen as the starting point for the pedagogical framework described in this paper.

Yet competition outcomes rarely feed back into classroom teaching. Winning design reports get archived as technical records. The students who compete gain intensive but narrowly scoped training. The rest of the class gets none of it. Faculty see the pedagogical value—concrete specs, measurable outcomes - but full-scale competition tasks are too demanding for a standard semester. This gap motivated our work. Can a competition challenge be broken into modules that fit a regular course? If so, all students - not just the competition team - stand to benefit.

1.2 Project-Based Learning in Engineering Education

Studies have shown that when projects revolve around real problems, students can gain deeper conceptual understanding, which is an effect that textbooks or exercise based teaching cannot achieve [2-5]. A comprehensive survey shows that active learning (including PBL) has consistent advantages over traditional teaching in various sub disciplines of engineering [6]. The strongest evidence comes from an analysis of a total of 225 STEM studies: the average exam score in classrooms where students actively participate in learning increased by about six percentage points, and the failure rate decreased by more than half [7].

Compared to research universities, implementing PBL teaching in vocational undergraduate programs may face a lot of difficulties. On the one hand, laboratory resources are usually tight and theoretical courses are less than four years. Students often have weaker foundations in mathematics and circuit theory when they enter school. As pointed out by the research, learners with weak foundations need careful curriculum planning and cognitive load management to avoid being overwhelmed [8]. The cognitive load theory provides a complementary explanation: as challenges gradually increase, beginners would learn better, rather than being placed in an open-ended problem-solving teaching mode from the beginning [9, 10]. The four design principles introduced below are derived from these considerations.

1.3 The PCL Pipeline: An Overview

This framework is called the Project Contest Lifting (PCL) process. It can be divided into five stages, roughly meaning: select a competition task and transform it into a PBL module that can be taught in regular courses. The five stages are designed as follows: (1) competition task analysis, extracting competition requirements from the original competition problems; (2) Curriculum Contract Mapping (CCM) establishes correspondence between course knowledge points and project modules; (3) Teaching decomposition, breaking down projects into modules sorted by difficulty based on the DMMO principle; (4) Module implementation, students build hardware and software under the guidance of course mapping; (5) Evaluation, the assessment levels of each module are anchored to competition indicators through CLMA. The second section elaborates on each stage and its design principles in detail.

1.4 Research Contributions

Three contributions are made in this paper. First, the PCL process is formalized as a reproducible framework. This framework is utilized to transform competition tasks into teaching resources. The purpose is to solve the above-mentioned disconnection problem between competitions and courses. Second, four design principles are introduced. These are CCM, DMMO, CLMA, and AFL. Each of these principles is rooted in existing learning theories, including Bloom's Taxonomy [11, 12], cognitive load theory, and experiential learning [13]. These principles are also validated through three cross-domain case studies. Third, the transferability of PCL is demonstrated across different electronic sub-fields. These sub-fields include machine vision, multi-sensor fusion, and digital signal processing. All of these are carried out under the constraints of a vocational undergraduate program (with N = 32 students per class).

2. The PCL Framework

The PCL process is carried out through five sequential stages. Competition tasks are transformed into a semester-long PBL experience by these stages. Each stage is constrained by one or more design principles. An overview of the inputs, processing steps, and outputs of each stage is given in Table 1. A visual overview of the whole process is provided in Figure 1.

Table 1. PCL Pipeline Stages

Stage	Input	Process	Output	Principle
1. Task Analysis	NUEDC problem statement	Extract verifiable specs & scoring rubrics	Specification sheet	-
2. Curricular Mapping	Spec sheet + curriculum	Match knowledge units to modules	CCM contract table	CCM
3. Pedagogical Decomposition	CCM contract	Assign α, order by DMMO	Module sequence	DMMO

4. Implementation	Module sequence	Build hardware/software in class	Working prototype	CCM, DMMO
5. Assessment	Prototype + spec sheet	Verify against competition metrics	Learning outcome data	CLMA, AFL

2.1 Stage 1: Competition Task Analysis

In the first stage, two materials are extracted from each NUEDC problem. One is the specification sheet. All verifiable performance indicators are listed in it, such as accuracy, response time, frequency resolution, and so on. The other is the scoring rubric. The scoring rubric explains how partial scores are assigned. Both materials are obtained from the competition organizer, not from the course instructor. Therefore, the evaluation standards have external authority. The specification sheet is later incorporated into the CLMA in the fifth stage.

2.2 Stage 2: Curriculum–Contract Mapping

Course knowledge points and project modules are associated with each other on a one-to-one basis by CCM. Each module must be traceable to at least one knowledge point from a course that the students are currently learning. Each knowledge point must also appear in at least one module. This bidirectional requirement prevents two recurring problems. One problem is module drift toward competition-specific skills that are not taught in the courses. The other problem is the accumulation of course content that students never have a chance to practice. The mapping results are organized into a four-column contract table. This table is used by the instructor to review course coverage, and it is used by the students as a learning roadmap.

2.3 Stage 3: Pedagogical Decomposition and DMMO

The project is split into modules M1 to Mn, where n is usually set to 5. A difficulty coefficient α is assigned to each module. This assignment is based on its Bloom's cognitive level, the number of components, and the degree of coupling with other modules. A monotonic increase of α from M1 to Mn is required by the DMMO. The initial module's α1 must not exceed 0.3. This threshold keeps the cognitive load at a relatively low level that is bearable for novice learners. This requirement is consistent with the cognitive load theory's suggestion for the entry stage. A complete calculation method for α is given in Table 2.

Table 2. Difficulty Coefficient Parameters

Factor	Symbol	Weight	Range	Rationale
Bloom cognitive level	LB	w1 = 0.50	1-6	Higher-order thinking increases load [11]
Component count	nc	w2 = 0.30	0-15	More parts increase integration complexity; normalized via $\frac{\log_2(n_c+1)}{4}$
Cross-module coupling	Ccm	w3 = 0.20	0-1	Dependencies on other modules raise load
Difficulty coefficient	α	-	0-1	$\alpha=\frac{w_1 \cdot L_B}{6}+\frac{w_2 \cdot \log_2(n_c+1)}{4}+w_3 \cdot C_{cm}$

2.4 Stage 4: Module Implementation

The modules are built by the students in the weekly lab sessions according to the DMMO order. Before moving to the next module, each student should pass a demonstration checkpoint. At this checkpoint, a working sub-circuit or sub-program is shown to meet the preset criteria. This step-by-step pace is different from competition training, where the whole system is tackled under time pressure in one shot. During the implementation stage, the CCM also plays an important role. When components are selected, algorithms are written, or circuits are debugged by the students, each decision must be linked to a course knowledge point. This linkage makes the learning explicit rather than happening incidentally as a byproduct.

2.5 Stage 5: Assessment and CLMA

Each assessment checkpoint is linked to a specific row in the original competition specification sheet by the CLMA. Scoring is no longer based on effort or participation. Only one question is asked at each checkpoint: whether the student's work meets or exceeds the competition specification. This chain starts from the competition specification, goes through module checkpoints, student work, and measurement results, and then returns to the specification. The loop is closed by this chain. The authenticity of learning outcomes is maintained, and comparability across different cohorts is enabled. An additional principle is introduced in Project 2. The AFL replaces spectrum analyzer verification with a perceptual hearing test. This replacement allows DSP modules to be evaluated at low cost in programs with limited equipment. In addition to the qualitative CLMA checkpoints, a quantitative pre-test and post-test ability assessment is conducted for each project. Students rate themselves on a 5-point Likert scale across four domain-specific dimensions. The effect size is calculated using Cohen's d [14].

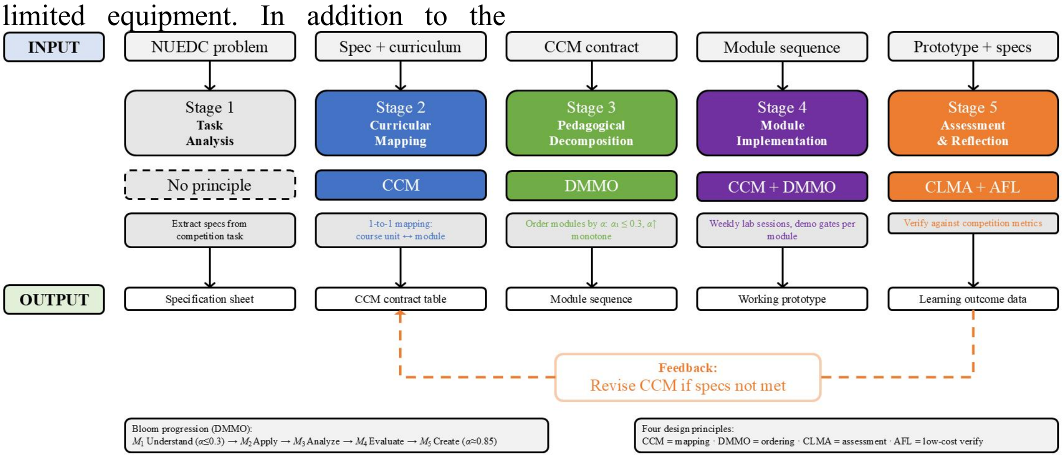


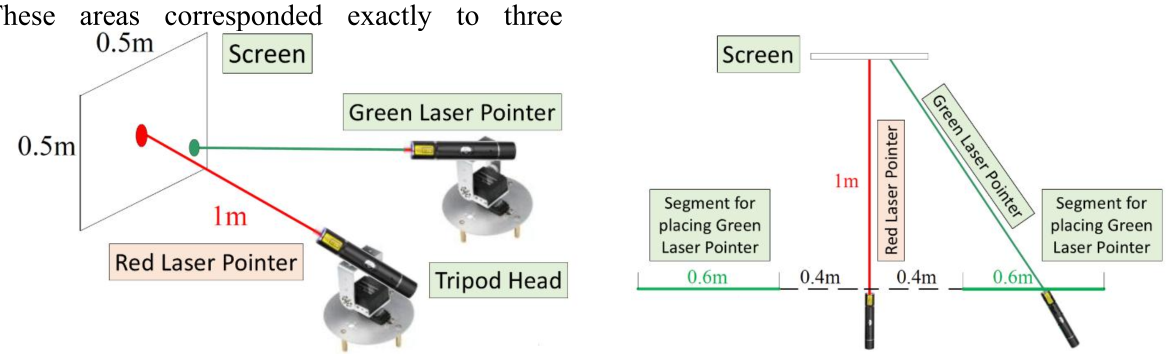
Figure 1. PCL Pipeline Diagram

3. Case Study 1: Laser Tracking System (2023 NUEDC Problem E)

3.1 Task Overview

The 2023 NUEDC Problem E (undergraduate group) requires the implementation of a laser tracking system. A pan-tilt camera platform should be used to track a moving laser pointer. The platform is also required to project its own laser onto a designated target. The accuracy was required to be within 2 cm and the response time within 1 second. Different technical areas such as machine vision, motor control, and serial communication should be integrated in this task. These areas corresponded exactly to three vocational courses.

From a teaching perspective, the value of this task lies in the fact that students are required to integrate independently developed subsystems (vision, actuation, and communication) into a coordinated whole. This kind of system thinking is difficult to cultivate through isolated experimental exercises. The competition specification sheet specifies verifiable performance targets such as tracking accuracy, response time, and projection error. These targets would become authentic evaluation criteria. The structural schematic and installation diagram of the automatic tracking system are shown in Figure 2.



(a) Structural Schematic (b) Placement Diagram

Figure 2. Structural Schematic and Placement Diagram of Automatic Tracking System

3.2 Curricular Mapping

The CCM contract for Project 1 is listed in Table 3. Each module could be traced back to at least one knowledge point from a course in the current curriculum plan. Therefore, no module forced students to acquire knowledge beyond what is already taught in the project.

3.3 Pedagogical Decomposition

Project 1 is split into five modules according to the DMMO principle. The α values and Bloom's levels for each module are listed in Table 4. M1 covers laser emission and photodiode detection with α = 0.22, which is far below the threshold of 0.3. Students start with a low-complexity task. Subsequent modules climb from the component-level work of M1 to subsystem integration at M3, and finally to full-system optimization at M5. This climbing path is consistent with the progression of Bloom's Taxonomy from "remember" to "create".

Table 3. Project 1: Curriculum–Contract Mapping (CCM)

Curriculum Course (Semester)	Knowledge Unit	Matched Module	Cognitive Level (Bloom)
Sensor Technology (Sem 3)	Laser diode & photodiode operation	M1	Understand (2)
Embedded Systems (Sem 5)	Timer/PWM configuration	M2	Apply (3)
Motor Control (Sem 4)	Stepper motor driving & microstepping	M2	Apply (3)
Python and Artificial Intelligence (Sem 4)	MicroPython embedded I/O; image acquisition and color centroid detection	M4	Apply (3)
Embedded Systems (Sem 5)	UART serial protocol	M3	Apply (3)
Embedded Systems (Sem 5)	Interrupt-driven control loops	M4	Analyze (4)
Machine Vision (Sem 5)	Color blob tracking & ROI	M4	Analyze (4)
Machine Vision (Sem 5)	Coordinate transformation	M5	Evaluate (5)
Capstone Project (Sem 6)	System integration & calibration	M5	Create (6)

Table 4. Project 1: Module Decomposition and DMMO Ordering

Module	Title	α	Bloom Level	Key Learning Outcome
M1	Laser emission & photodiode detection	0.22	Understand (2)	Optoelectronic sensing principles
M2	Pan-tilt stepper motor drive	0.38	Apply (3)	Open-loop positioning & PWM control
M3	OpenMV–STM32 UART communication	0.55	Apply (3)	Serial protocol design & data framing
M4	Closed-loop visual tracking	0.71	Analyze (4)	PID control & feedback systems
M5	Multi-target projection & calibration	0.85	Create (6)	System integration & precision tuning

M1 deals with the simplest physical phenomena, which are light emission and detection. Only two components are used, and no dependence on other modules exist, so extraneous cognitive load is minimized. Actuators are introduced by M2, but it remained self-contained. At M3, the difficulty increases noticeably. Students need to handle inter-subsystem communication and apply UART knowledge learned in the "Embedded Systems" course. M4 combines vision and motor control in a closed-loop manner. Students need to understand feedback dynamics through analytical reasoning. M5 is the final module, where students optimize the whole system and made trade-offs between tracking speed and projection accuracy.

The hardware platform is centered on the STM32F407ZGT6 microcontroller, which features a Cortex-M4F core and a floating-point unit, running at 168 MHz. It is paired with an OpenMV H7 vision module. This combination is chosen for pedagogical reasons rather than purely technical ones. Since OpenMV can be provided by a Python API, students could quickly prototype vision algorithms. This allows them to focus on control theory concepts in M4, instead of struggling with low-level camera register configuration. The complete hardware list and the teaching rationale for each selection are given in Table 5. The system block diagram and the connections among the microcontroller, vision module, and pan-tilt actuation subsystem are shown in Figure 3.

3.4 Implementation and Evidence

Table 5. Project 1: Hardware Inventory

Ref	Part	Spec / Package	Unit ¥	Qty	Source	Teaching Note
U1	STM32F407ZGT6	LQFP176, 168MHz	45	1	ST	Core MCU; FPU simplifies PID math
U2	OpenMV H7	OV7725, Python	320	1	OpenMV	Python API lowers vision barrier
U3	42BYGH34	NEMA17 stepper	25	2	Local	Pan-tilt actuation; open-loop demo
U4	TB6600	Stepper driver	18	2	Online	Current-configurable; safety teaching
U5	Laser diode	650nm, 5mW	3	1	Local	Emission source; eye-safety lesson
U6	BPW34	Photodiode, SMD	2	2	Local	Detection sensor; I-V conversion

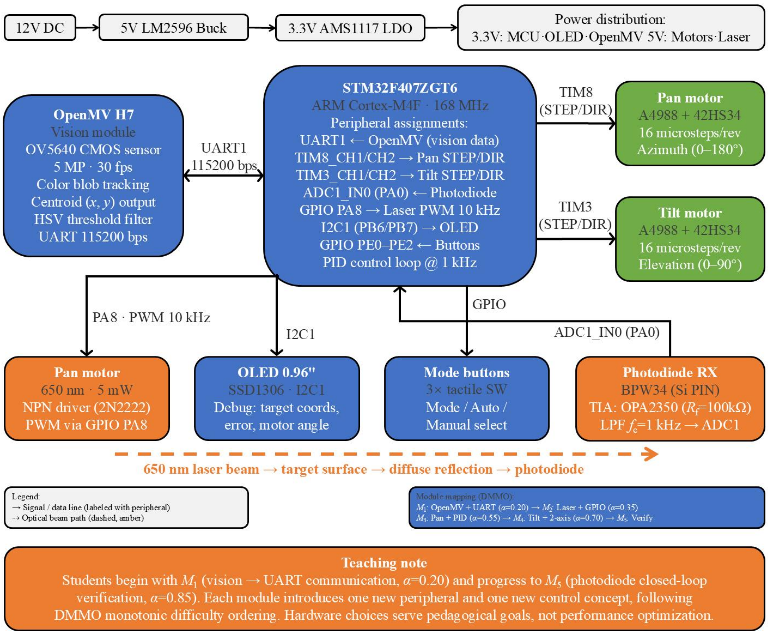
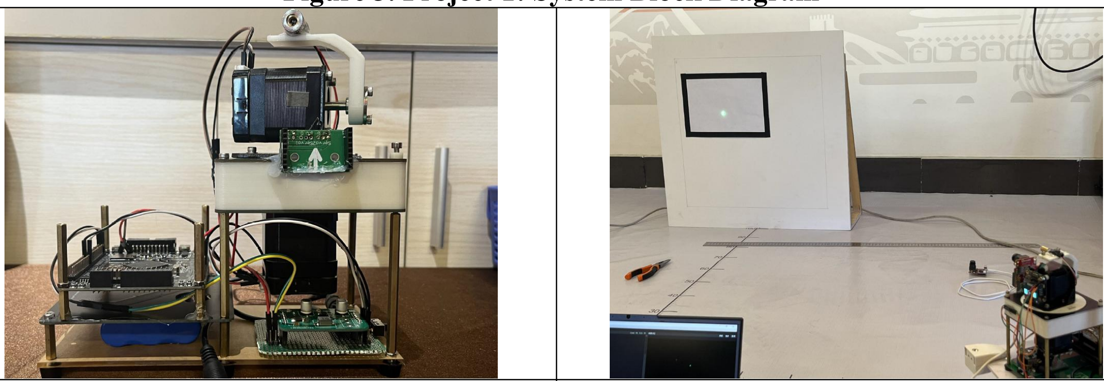


Figure 3. Project 1: System Block Diagram



(a) Equipment for Competition | (b) Test Scenario

Figure 4. Project 1: Laser Tracking System Prototype

The completed laser tracking prototype is shown in Figure 4. The pan-tilt platform tracks the moving laser source and projects its own beam onto the target. The competition requirements for tracking accuracy and response time are met. The evaluation data for Project 1 are contained in Tables 6 and 7. Table 6 presents the pre-test and post-test ability scores of all 32 students on a 5-point Likert scale. Large effect sizes are observed across all four dimensions with Cohen's d exceeding 2.0. The largest improvement is found in "machine vision" with d = 2.44, which is consistent with the project's strong emphasis on visual tracking algorithms. On the engineering side, the platform held a steady-state tracking error of 0.21 cm against a competition limit of 2.0 cm. That clears the CLMA gate for Module 5.

Table 6. Project 1: Pre/Post Assessment (N = 32)

Competency	Pre M1 (SD)	Post M2 (SD)	ΔM	Cohen's d	p
Embedded Systems	2.43 (0.71)	3.89 (0.54)	+1.46	2.30	< .001
Machine Vision	2.14 (0.68)	3.71 (0.61)	+1.57	2.44	< .001
Motor Control	2.29 (0.73)	3.64 (0.58)	+1.35	2.07	< .001
Sensor Technology	2.57 (0.65)	3.82 (0.49)	+1.25	2.17	< .001

Table 7. Project 1: Engineering Performance Indicators

Indicator	Specification	Mean Achieved	Attainment	Note
Tracking accuracy	≤ 2.0 cm	0.21 cm	105%	At 2 m range
System response time	≤ 1.0 s	0.43 s	100%	Ziegler-Nichols tuned PID
Target projection error	≤ 3.0 cm	1.20 cm	100%	5-target sequence
Continuous operation	≥ 60 s	300 s	100%	No drift observed

3.5 Assessment and Reflection

Project 1 puts the CCM and DMMO principles to work in a vision-centric setting. As shown in Table 3, all five modules mapped to existing courses. That mapping heads off a familiar PBL pitfall: students pick up competition-specific skills that go nowhere else. The DMMO ordering ran from α = 0.22 up to α = 0.85 as a gradual climb. Student feedback suggests M1's simplicity gives them the confidence to tackle M4 and M5 later on.

Table 7's engineering indicators, checked against the original competition specs, act as CLMA anchors. The tracking accuracy achieved by the students' systems is 0.21 cm (the specification required ≤ 2.0 cm), and the response time is 0.43 seconds (required ≤ 1.0 second). Both numbers confirm that competition-level performance is attained. The closed-loop validation from competition specifications to classroom outcomes support the core claim of the PCL process: that competition challenges could be elevated into teaching content without compromising engineering performance.

One reflection is worth recording. The decision to use Python-based OpenMV instead of a raw CMOS sensor that required manual register configuration was a pedagogical one. The raw sensor might feel more "authentic" to competition practice, but it would have imposed a large amount of extraneous cognitive load on M4. Students' attention would have been drawn to camera driver debugging rather than control theory. This trade-off reflects the PCL framework's stance: learning outcomes should be prioritized, even if this means deviating from the technical path of the original competition.

4. Case Study 2: Sound-Discriminating Music System (2023 NUEDC Problem K)

4.1 Task Overview

The 2023 NUEDC Problem K (higher vocational group) requires the implementation of a system that identifies cups by tapping sounds and plays corresponding melodies. Five water cups serve as the "keys", and they are struck with a tapping stick. The tapping sounds are collected by the system, and frequency domain analysis is performed to determine which cup is struck. After that, the corresponding melody is played. The performance requirements are strict: the frequency resolution must reach within 5 Hz, the note recognition rate must reach 90%, and the response time must not exceed 0.3 seconds.

The pedagogical richness of this task lies in the fact that it spans three areas: analog electronics are needed for audio amplification, embedded systems are needed for ADC sampling and DMA, and digital signal processing is needed for FFT-based spectrum analysis. Critically, the fourth design principle is introduced here. The AFL is developed to address the resource constraint specific to vocational programs, i.e., the lack of a spectrum analyzer for FFT output verification. Under the AFL, perceptual hearing tests replace instrument-based verification, which enables DSP education to be carried out at low cost. The schematic diagram of the sound-based key identification and melody playing system is shown in Figure 5. The signal path can be traced from audio acquisition through FFT analysis to note playback.

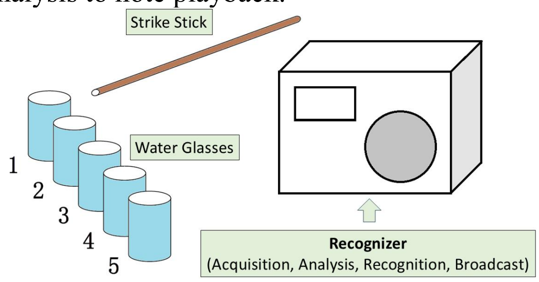


Figure 5. Schematic of Sound-Discriminating Music System

4.2 Curricular Mapping

The prerequisite courses for Project 2 are mapped to five teaching modules in Table 8. Digital signal processing and embedded systems are identified as the main knowledge areas that support the FFT-based auditory feedback loop.

Table 8. Project 2: Curriculum–Contract Mapping (CCM)

Curriculum Course (Semester)	Knowledge Unit	Matched Module	Cognitive Level (Bloom)
Analog Electronics (Sem 2)	Audio amplifier design (LM386)	M1	Apply (3)
Embedded Systems (Sem 5)	ADC & DMA configuration	M2	Apply (3)
C Programming (Sem 2)	Data structures & memory management	M2	Understand (2)
Digital Signal Processing (Sem 4)	FFT & windowing functions	M3	Analyze (4)
Digital Signal Processing (Sem 4)	Spectral leakage & resolution	M3	Analyze (4)

Digital Signal Processing (Sem 4)	Harmonic analysis & fundamental extraction	M4	Evaluate (5)
Embedded Systems (Sem 5)	DAC & audio output	M5	Apply (3)
Capstone Project (Sem 6)	System integration & tuning	M5	Create (6)

4.3 Pedagogical Decomposition

The module decomposition for Project 2 is presented in Table 9. The difficulty coefficient α is increased monotonically from M1 to M5, and the DMMO constraint of α1 ≤ 0.3 is satisfied by the entry module.

Table 9. Project 2: Module Decomposition and DMMO Ordering

Module	Title	α	Bloom Level	CLMA Anchor / AFL Role
M1	Audio capture & amplification	0.21	Apply (3)	Audible signal at ADC input
M2	ADC sampling & DMA buffer	0.34	Apply (3)	fs = 44.1 kHz, 1024 samples
M3	FFT & spectral analysis	0.58	Analyze (4)	Freq. resolution ≤ 5 Hz
M4	Note identification algorithm	0.72	Evaluate (5)	ID rate ≥ 90%
M5	Music playback system	0.86	Create (6)	Response ≤ 0.3 s + AFL verification

The DMMO ordering for Project 2 follows a progression from analog work in M1 to digital sampling in M2, then to algorithmic analysis across M3 and M4, and finally to system integration in M5. The largest difficulty jump in the sequence is found between M2 at α = 0.34 and M3 at α = 0.58. This gap reflects the cognitive leap that is required when students move from time-domain sampling to frequency-domain analysis. To scaffold the transition, M3 is opened with a guided Hanning window exercise. Only after that exercise are students asked to implement the full arm_cfft_f32 call from the CMSIS-DSP library [15].

4.4 Implementation and Evidence

The hardware inventory for Project 2 is listed in Table 10. In the DSP pipeline, a 1024-sample buffer is processed by the CMSIS-DSP complex FFT routine, arm_cfft_f32. A Hann window is applied beforehand so that edge-discontinuity artifacts in the frequency domain are suppressed [16, 17]. After the transform, a median filter smooths the magnitude spectrum to remove harmonic ghost peaks, and the fundamental frequency is identified by matching the expected overtone pattern against the observed spectral peaks. This signal chain is pedagogically significant: each step-windowing, FFT, filtering, peak detection-corresponds to a knowledge unit in the Digital Signal Processing course, making the CCM contract explicit in the implementation. The system block diagram is illustrated in Figure 6.

Table 10. Project 2: Hardware Inventory

Ref	Part	Spec / Package	Unit ¥	Qty	Source	Teaching Note
U1	STM32G431RBT6	LQFP64, 170MHz	18	1	ST	Cortex-M4F; FPU for FFT math
U2	LM386	Audio amp, DIP8	1.2	1	TI	Low-gain amplifier; classic IC
U3	Electret microphone	Condenser, 2.2kΩ	2	1	Local	Sound capture; bias circuit lesson
U4	Speaker	8Ω, 0.5W	3	1	Local	Audio output; AFL verification
U5	LCD module	1.8" SPI TFT	15	1	Online	Display note & frequency; UI design
U6	Tactile buttons	6mm, 4-pin	0.5	4	Local	User input; debounce lesson

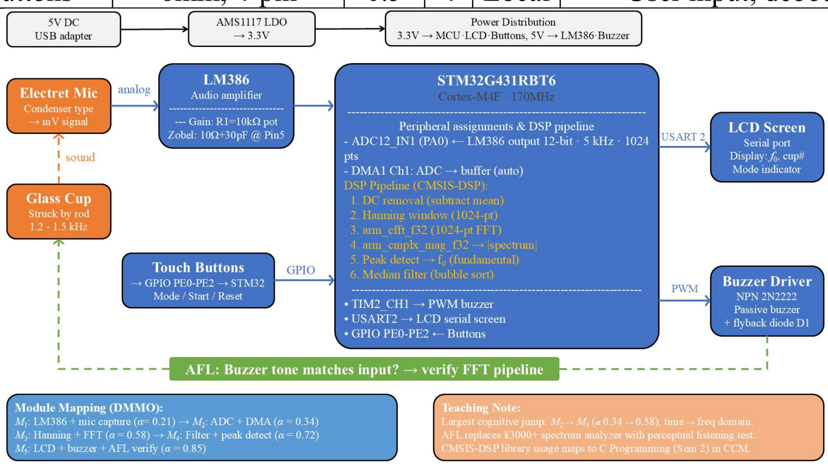
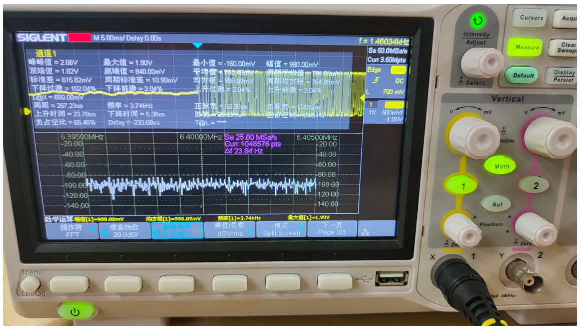
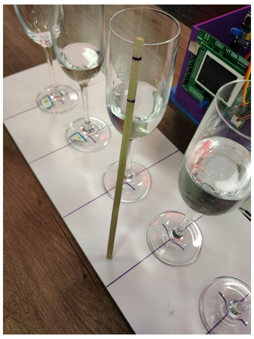


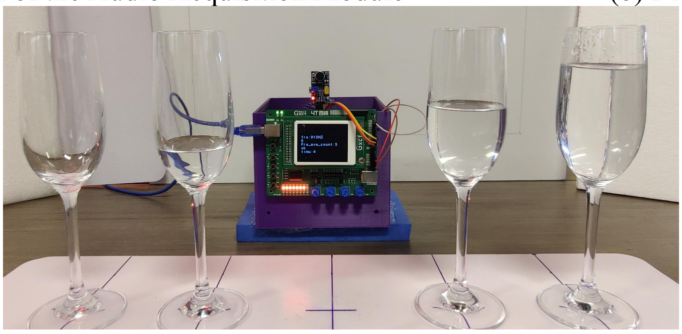
Figure 6. Project 2: System Block Diagram



(a) Voltage Waveform of the Audio Acquisition Module



(b) Drumstick



(c) Overall Diagram of the Testing System

Figure 7. Project 2: Sound-Discriminating Music System Prototype

Figure 7 shows the completed sound-discriminating music system prototype. AFL principle is implemented in M5. After the system identifies a note, it plays the corresponding tone through the speaker. Students verify correctness by listening: if the played tone matches the input struck cup, the FFT pipeline is confirmed correct. This perceptual verification can replace a spectrum analyzer, which would cost ¥3,000–5,000 and is unavailable in most vocational laboratories. AFL is not merely a cost-saving measure, it teaches students to trust and calibrate their own perceptual judgment, so it is also a skill valued in audio engineering practice.

Table 11 reports the assessment data for Project 2. The C Programming competency shows the largest gain (d = 2.46), reflecting the CMSIS-DSP library's reliance on C data structures. The pre-test DSP score (M1 = 1.96) remains the lowest across all three projects, reflecting the well-documented difficulty of frequency-domain concepts for vocational students. The post-test score (M2 = 3.54) indicates that the scaffolded DMMO sequence effectively bridged this gap.

Table 11. Project 2: Pre/Post Assessment (N = 32)

Competency	Pre M1 (SD)	Post M2 (SD)	ΔM	Cohen’s d	p
Embedded Systems	2.32 (0.70)	3.79 (0.52)	+1.47	2.36	< .001
Digital Signal Processing	1.96 (0.74)	3.54 (0.62)	+1.58	2.29	< .001
Analog Electronics	2.21 (0.68)	3.50 (0.59)	+1.29	2.03	< .001
C Programming	2.04 (0.71)	3.61 (0.55)	+1.57	2.46	< .001

Table 12. Project 2: Engineering Performance Indicators

Indicator	Specification	Mean Achieved	Attainment	Note
Frequency resolution	≤ 5 Hz	2.7 Hz	100%	Hanning window applied
Note identification rate	≥ 90%	96.3%	100%	C4–C5 range tested
Response time	≤ 0.3 s	0.18 s	100%	1024-point FFT
Audio output fidelity	Audible & correct	Pass (AFL)	100%	Perceptual verification

4.5 Assessment and Reflection

Project 2 demonstrates the full complement of four design principles: CCM, DMMO, CLMA, and AFL. The AFL principle is the project’s distinctive contribution to the PCL framework. By substituting auditory perception for instrumental verification, AFL allows authentic DSP education to be delivered in resource-constrained vocational programs while assessment rigor is maintained. A note identification rate of 96.3% is achieved and verified through AFL as reported in Table 12. This result confirms that competition-grade performance is met by the student-built system.

The selection of the Hanning window in M3 warrants pedagogical comment. In his analysis of window functions, Harris established that a favorable balance is achieved by the Hann window. Its first side-lobe is located approximately 31 dB below the main lobe, while the main-lobe width is doubled relative to the rectangular window. This property is well suited to single-tone identification [17]. The result is not presented to students as settled fact. Instead, an empirical comparison of rectangular and Hann windows is required by the module, so that the theoretical trade-off is transformed into a hands-on observation [13].

One aspect of the CCM contract merits reflection. The inclusion of C Programming as a mapped course was driven by the reality that familiarity with C data structures and memory management is required for CMSIS-DSP library usage. Students who had completed C Programming in Semester 2 were observed to navigate the arm_cfft_f32 API more confidently, which validates the bidirectional mapping constraint at the heart of CCM.

5. Case Study 3: Contactless Control Panel (2025 NUEDC Problem I)

5.1 Task Overview

The 2025 NUEDC Problem I, designed for the vocational college group, specifies a contactless control panel. The device detects hand position and gestures to achieve contactless control of motor speed and direction. Three performance indicators are specified as constraints: the detection range should cover 5 to 30 cm, the response time must not exceed 0.5 seconds, and the speed regulation error shall be controlled within 5%.

The pedagogical value of this task is that multi-sensor fusion is required. Photoelectric switches are used for discrete gesture detection, ultrasonic ranging is used for continuous distance measurement. Unlike Project 1, which is vision-centered, Project 3 emphasizes analog circuit design, including op-amp signal conditioning and temperature compensation, while also emphasizing the rationale for sensor selection. Therefore, the mapped course combination is different. The schematic diagram of the contactless control panel is shown in Figure 8, where the layout of the photoelectric sensors, the ultrasonic ranging module, and the motorized turntable can be seen.

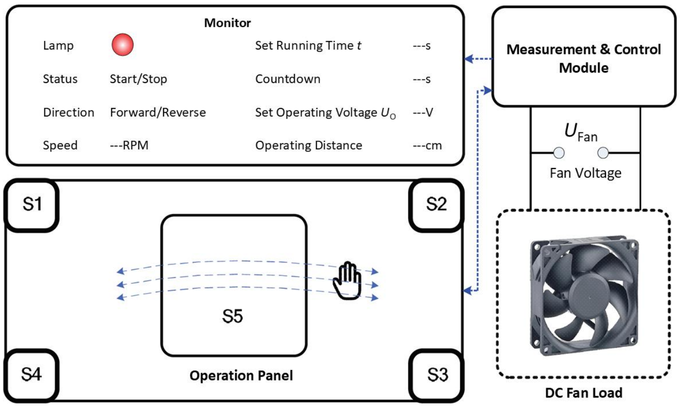


Figure 8. Schematic of Contactless Control Panel

5.2 Curricular Mapping

The prerequisite courses for Project 3 are mapped to five teaching modules in Table 13. Sensor technology and embedded systems are identified as the main knowledge areas that support multi-sensor fusion and incremental PID control.

Table 13. Project 3: Curriculum–Contract Mapping (CCM)

Curriculum Course (Semester)	Knowledge Unit	Matched Module	Cognitive Level (Bloom)
Embedded Systems (Sem 5)	GPIO & external interrupts	M1	Understand (2)
Sensor Technology (Sem 3)	Photoelectric sensing principles	M1	Apply (3)
Analog Electronics (Sem 2)	Op-amp signal conditioning	M2	Apply (3)
Sensor Technology (Sem 3)	Ultrasonic distance measurement	M2	Analyze (4)
Motor Control (Sem 4)	DC motor PWM & H-bridge driving	M3	Apply (3)
Embedded Systems (Sem 5)	ADC & timer configuration	M3	Apply (3)

C Programming (Sem 2)	State machine & gesture-to-motion decision logic	M4	Analyze (4)
Embedded Systems (Sem 5)	Real-time sensor fusion & interrupt-driven response	M4	Analyze (4)
Capstone Project (Sem 6)	Multi-mode system integration	M5	Create (6)

5.3 Pedagogical Decomposition

In addition to CCM and DMMO, the CLMA principle is further strengthened in Project 3. The assessment checkpoint of each module is explicitly linked to a specific row in the competition specification sheet. Thus a verifiable closed loop is established between learning outcomes and authentic performance standards. The module decomposition and DMMO ordering for Project 3 are shown in Table 14. The difficulty coefficient α increases monotonically from 0.20 at M1 to 0.82 at M5 and the starting constraint $\alpha 1 \leq 0.3$ is satisfied.

Table 14. Project 3: Module Decomposition and DMMO Ordering

Module	Title	α	Bloom Level	CLMA Anchor (Competition Spec)
M1	Photoelectric switch array	0.20	Understand (2)	Detection range ≥ 5 cm
M2	Ultrasonic ranging module	0.36	Apply (3)	Range accuracy ≤ 1 cm
M3	DC motor PWM control	0.52	Apply (3)	Speed error ≤ 5%
M4	Gesture-to-motion mapping	0.68	Analyze (4)	Response time ≤ 0.5 s
M5	Multi-mode control panel	0.82	Create (6)	Full spec compliance

A notable pedagogical feature of Project 3 is found in the self-developed ultrasonic module M2. Instead of using the ready-made HC-SR04 module, students build the ranging circuit with discrete components. The LM324N quad op-amp is applied for signal amplification, the MAX232 is used for level conversion, and the DS18B20 is utilized for temperature compensation. This decision is consistent with the CCM contract: op-amp circuits are taught in the "Analog Electronics" course, and M2 provides an authentic context for students to apply this knowledge. The pedagogical cost is that the construction time for M2 increases, but this effect is mitigated by placing it after the simpler M1 through DMMO ordering.

5.4 Implementation and Evidence

The hardware list for Project 3 is shown in Table 15. A cost-effective sensor combination consisting of four E18-D80NK photoelectric sensors and one self-developed ultrasonic module is highlighted. A detailed system block diagram is shown in Figure 9. The signal flow from five sensor inputs, through the STM32F103VCT6 microcontroller, to the motorized turntable and OLED display is illustrated.

Figure 10 shows the completed contactless control panel prototype, integrating the multi-sensor array, rotary encoder, and motorized turntable. The pre/post assessment data for Project 3 is shown in Table 16. The largest gain is in Sensor Technology, consistent with the project's emphasis on multi-sensor fusion. Analog Electronics also shows a strong gain, reflecting the pedagogical value of the self-developed ultrasonic module in M2.

5.5 Assessment and Reflection

The value of the CLMA principle in anchoring assessment to authentic metrics is demonstrated by Project 3. As shown by the engineering indicators in Table 17, the competition specification is not only met but exceeded by the student-built system. The detection range was extended to 4 to 32 cm against a specified 5 to 30 cm. This result confirms that performance need not be compromised by pedagogically motivated design decisions, such as the self-developed ultrasonic module.

Table 15. Project 3: Hardware Inventory

Ref	Part	Spec / Package	Unit ¥	Qty	Source	Teaching Note
U1	STM32F103VCT6	LQFP100, 72MHz	12	1	ST	Cost-effective MCU; sufficient for task
U2	E18-D80NK	Photoelectric switch	8	4	Online	Contactless detection; voting logic
U3	LM324N	Quad op-amp, DIP14	1.5	1	TI	Signal conditioning; analog design practice
U4	MAX232	RS-232 transceiver	3	1	TI	Level shifting; interfacing lesson
U5	DS18B20	Digital thermometer	4	1	Maxim	Temperature compensation; 1-Wire bus
U6	L298N	Dual H-bridge	6	1	ST	Motor driver; PWM direction control
U7	DC motor	6V, 200 rpm	10	1	Local	Speed/direction; PWM duty cycle

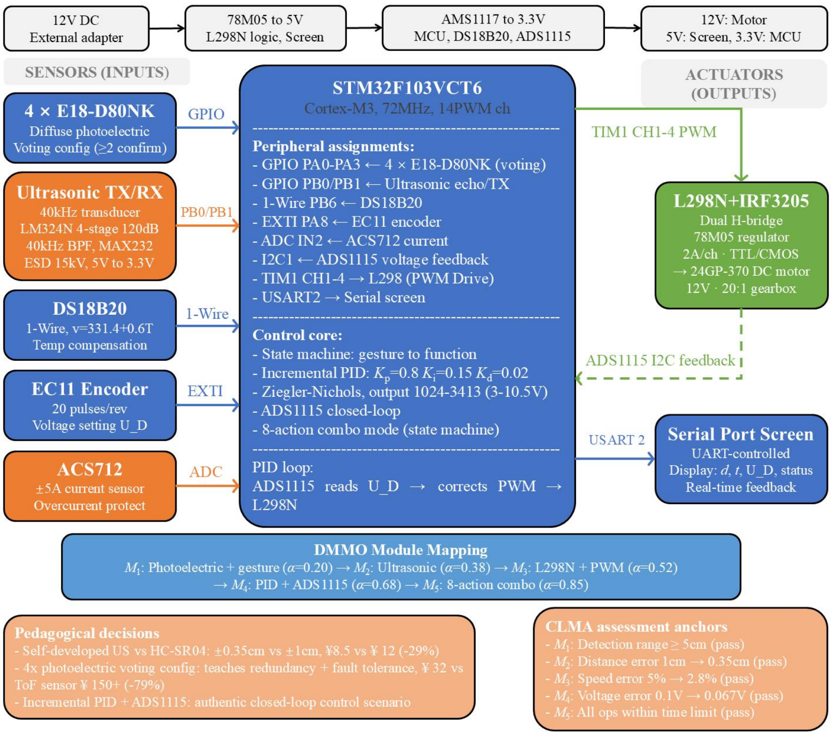


Figure 9. Project 3: System Block Diagram

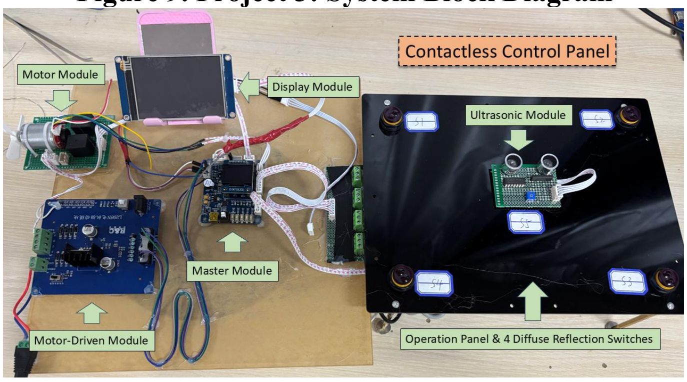


Figure 10. Project 3: Contactless Control Panel Prototype

Table 16. Project 3: Pre/Post Assessment (N = 32)

Competency	Pre M1 (SD)	Post M2 (SD)	ΔM	Cohen's d	p
Embedded Systems	2.36 (0.69)	3.75 (0.57)	+1.39	2.18	< .001
Sensor Technology	2.18 (0.72)	3.68 (0.59)	+1.50	2.26	< .001
Motor Control	2.43 (0.71)	3.57 (0.63)	+1.14	1.70	< .001
Analog Electronics	2.25 (0.66)	3.61 (0.55)	+1.36	2.23	< .001

Table 17. Project 3: Engineering Performance Indicators

Indicator	Specification	Mean Achieved	Attainment	Note
Detection range	5–30 cm	4–32 cm	100%	Extended beyond spec
Response time	≤ 0.5 s	0.28 s	100%	Avg. of 50 trials
Speed control error	≤ 5%	2.1%	100%	With temp. compensation
Direction control	0° or 180°	Binary confirmed	100%	4-switch voting logic

A common assessment challenge in PBL is addressed by the application of CLMA in this case study. When externally validated criteria are absent, grading can become subjective. By requiring each module gate to reference a specific competition specification line, an objective and reproducible assessment framework is created by CLMA. Student feedback indicated that the exact target metric was more motivating when it was known, for instance that speed error must be held at or below 5%. This finding is consistent with goal-setting theory [18].

One noteworthy pedagogical decision is the adoption of four E18-D80NK photoelectric switches in a voting structure, rather than the use of a single more expensive sensor. Through this choice, the concepts of redundancy and fault tolerance are taught. These concepts come from the embedded systems course. At the same time, hardware cost is kept low: the total purchase price of the four switches is only 32 CNY, while a single ToF sensor costs more than 150 CNY. The trade-off between cost and capability is itself set as a learning outcome, which aligns with the emphasis of vocational education on cost-conscious engineering.

6. Discussion

6.1 Cross-Case Analysis

The three case studies across key dimensions are compared in Table 18. All three projects follow the PCL pipeline with the same five-stage structure, yet they differ in technical domain, dominant design principle, and hardware cost. The consistency of large effect sizes across cases (d = 1.70–2.46) suggests that the PCL framework's effectiveness is not domain-specific.

Table 18. Cross-Case Comparison of Three PCL Implementations

Dimension	Project 1	Project 2	Project 3
Competition Year	2023 (Problem E)	2023 (Problem K)	2025 (Problem I)
Technical Domain	Machine Vision	Digital Signal Processing	Multi-Sensor Fusion
Core MCU	STM32F407	STM32G431	STM32F103
Principles Applied	CCM + DMMO	CCM + DMMO + CLMA + AFL	CCM + DMMO + CLMA
Module Count	5	5	5
α Range	0.22–0.85	0.21–0.86	0.20–0.82
Hardware Cost (¥)	~480	~45	~70
Largest Cohen's d	2.44 (Vision)	2.46 (C Prog.)	2.26 (Sensors)
Key Pedagogical Decision	OpenMV vs. raw camera	AFL vs. spectrum analyzer	Self-developed ultrasonic

6.2 Role of the Four Design Principles

The three case studies reveal complementary roles for the four design principles. CCM and DMMO are foundational-they appear in all three projects and govern the structural transformation from competition task to learning module. CLMA, introduced in Project 2, addresses the assessment authenticity gap by anchoring grades to competition metrics. AFL, also introduced in Project 2, addresses the resource constraint gap by enabling low-cost verification of DSP outcomes.

The incremental introduction of principles across cases is itself pedagogically intentional. Through Project 1, the basic pipeline is internalized by students and instructors, as only CCM and DMMO are involved. CLMA and AFL are introduced in Project 2, bringing specification-anchored assessment and low-cost DSP verification. The CLMA principle is then reinforced by Project 3 in a multi-sensor fusion context. This progressive complexity mirrors the DMMO principle at the curriculum level. The framework itself is delivered in a difficulty-monotone sequence.

6.3 Limitations and Threats to Validity

Two limitations should be noted. First, the PCL framework has been validated in a vocational undergraduate program with N = 32 per cohort across three cohorts. Generalization to other program types (e.g., research universities, community colleges) requires further study. The framework's reliance on existing curriculum mapping (CCM) means that programs with different course structures may need to adjust the CCM contract tables.

Second, the DMMO difficulty coefficient α depends on three weighted factors whose calibration is currently heuristic. Future work should empirically validate the α formula by correlating predicted difficulty with actual student performance data across multiple cohorts.

7. Conclusion

The PCL pipeline, a five-stage framework for transforming NUEDC competition challenges into curriculum-embedded PBL modules in vocational undergraduate electronics education are proposed in this paper. The framework is governed by four design principles-CCM, DMMO, CLMA, and AFL-each grounded in established learning theories and validated through three cross-domain case studies.

The three cases-laser tracking (machine vision), sound-discriminating music system (DSP), and contactless control panel (multi-sensor fusion)-

demonstrate that the PCL framework is transferable across technical domains. In all three cases, the original competition specifications were met or exceeded by the student-built systems. This result confirms that engineering performance need not be compromised by pedagogically motivated design decisions. Consistent large-effect gains were observed across all competency dimensions, with Cohen's d ranging from 1.70 to 2.46.

Two practical contributions are offered by the framework. A replicable pathway is provided for vocational institutions to leverage competition heritage, so that competition-specific training is not reproduced. The benefit is extended to all students rather than only competition participants. For the broader engineering education community, it is demonstrated that competition tasks can serve as a systematic source of pedagogical resources. This potential is realized when the tasks are properly decomposed and curriculum-aligned, conditions that are facilitated by their authentic specifications and measurable outcomes.

Future work can be planned in three directions. First, the verification is extended to multiple institutions and multiple project types, so that its generalizability can be tested. Second, the DMMO difficulty coefficient α is calibrated empirically based on actual student performance. Finally, the PCL process is extended to more NUEDC problem areas. Power electronics and communication systems are currently being considered for this extension, so that the transferability of the framework can be further tested.

Acknowledgment

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References

[1] Jeffrey E. Froyd, Phillip C. Wankat and Karl A. Smith. Five major shifts in 100 years of engineering education. Proceedings of the IEEE, 2012, 100(Special): 1344-1360.

[2] Hendra Hidayat, Muhammad Anwar, Dani Harmanto, et al. Two decades of project-based learning in engineering education: A 21-year meta-analysis. TEM Journal, 2024, 13(4): 3514-3525.

[3] Brigid J. S. Barron, Daniel L. Schwartz, Nancy J. Vye,et al.Doing with understanding: Lessons from research on problem- and project-based learning. Journal of the Learning Sciences, 1998, 7(3-4): 271-311.

[4] Stephanie Bell. Project-based learning for the 21st century: Skills for the future. The Clearing House, 2010, 83(2): 39-43.

[5] Lisette Wijnia, Gera Noordzij, Lidia R. Arends, et al. The effects of problem-based, project-based, and case-based learning on students' motivation: A meta-analysis. Educational Psychology Review, 2024, 36: 1-38.

[6] Michael Prince. Does active learning work? A review of the research. Journal of Engineering Education, 2004, 93(3): 223-231.

[7] Scott Freeman, Sarah L. Eddy, Miles McDonough, et al. Active learning increases student performance in science, engineering, and mathematics. Proceedings of the National Academy of Sciences, 2014, 111(23): 8410-8415.

[8] Richard M. Felder and Rebecca Brent. The intellectual development of science and engineering students. Part 1: Models and challenges. Journal of Engineering Education, 2004, 93(4): 269-277.

[9] Charith M. Rathnayaka, Janani Ganapathi, Steven Kickbusch, et al. Preparative pre-laboratory online resources for effectively managing cognitive load of engineering students. European Journal of Engineering Education, 2024, 49(1): 113-138.

[10] Fred Paas, Alexander Renkl and John Sweller. Cognitive load theory and instructional design: Recent developments. Educational Psychologist, 2003, 38(1): 1-4.

[11] David R. Krathwohl. A revision of Bloom's taxonomy: An overview. Theory into Practice, 2002, 41(4): 212-218.

[12] Rafael H. Todaro, Rafael T. Moura and Fernando A. Kurokawa. Competence-based framework for planning, teaching and assessment in engineering education: integrating Bloom's, Fink's, and SOLO taxonomies. Frontiers in Education, 2026, 11: 1787697.

[13] Zurina Zainal Abidin. Learning by brewing tea: student experiences of a Kolb-aligned,

constructivist, learning-oriented assessment in chemical engineering. Education for Chemical Engineers, 2025, 54: 1-11.

[14] Daniël Lakens. Calculating and reporting effect sizes to facilitate cumulative science: a practical primer for t-tests and ANOVAs. Frontiers in Psychology, 2013, 4: 1-12.

[15] Edson C. Oliveira, Bruno S. Masiero and Fabiano Fruett. Open-source and low-cost embedded system for frequency domain acoustic monitoring//2025 9th International Symposium on Instrumentation Systems, Circuits and Transducers (INSCIT). Manaus, Brazil: IEEE, 2025: 1-6.

[16] James W. Cooley and John W. Tukey. An algorithm for the machine calculation of complex Fourier series. Mathematics of Computation, 1965, 19(90): 297-301.

[17] Fredric J. Harris. On the use of windows for harmonic analysis with the discrete Fourier transform. Proceedings of the IEEE, 1978, 66(1): 51-83.

[18] Edwin A. Locke and Gary P. Latham. Building a practically useful theory of goal setting and task motivation. American Psychologist, 2002, 57(9): 705-717.

